Planare elektrostatisch dotierte rekonfigurierbare Schottky-Barriere FDSOI Feldeffekttransistor Strukturen

Planar Electrostatically Doped Reconfigurable Schottky Barrier FDSOI Field-Effect Transistor Structures

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
genehmigte Dissertation von Tillmann A. Krauss aus Offenbach am Main
Tag der Einreichung: 27.09.2018, Tag der Prüfung: 26.04.2019
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1. Gutachten: Prof. Dr. rer. nat. Udo Schwalke
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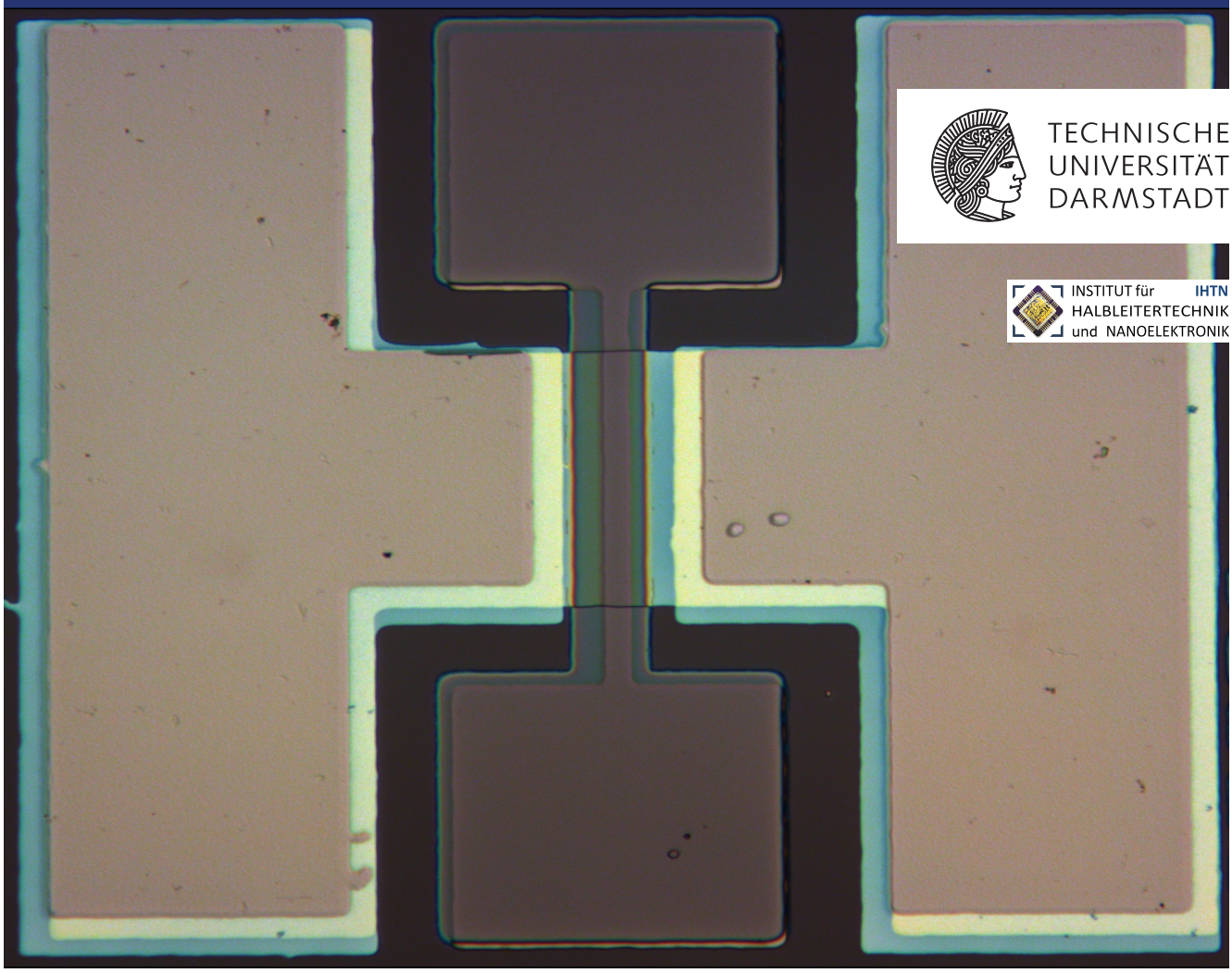

TECHNISCHE UNIVERSITÄT DARMSTADT

INSTITUT für IHTN HALBLEITERTECHNIK und NANOELEKTRONIK

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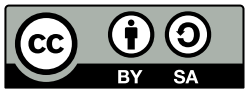

TECHNISCHE UNIVERSITÄT DARMSTADT

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Vom Fachbereich Elektrotechnik und Informationstechnik
der Technischen Universität Darmstadt

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Doktor-Ingenieurs (Dr.-Ing.)

genehmigte Dissertation

von

Dipl.-Wirtsch.-Ing. Tillmann A. Krauss

geboren am 24. Januar 1981 in Offenbach am Main

Referent:	Prof. Dr. rer. nat. Udo Schwalke
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TECHNISCHE UNIVERSITÄT DARMSTADT

Erklärung laut §9 PromO

Ich versichere hiermit, dass ich die vorliegende Dissertation selbstständig und nur unter Verwendung der angegebenen Literatur verfasst habe. Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient.

(Tillmann A. Krauss)
Darmstadt, den 27.09.2018

Kurzfassung

Unsere Wirtschaft sowie auch unsere Gesellschaft wurden in den vergangenen 50 Jahren durch elektronische Innovationen maßgeblich geprägt. Dieser große Einfluss der Elektronik basiert insbesondere auf deren kontinuierlichen Verbesserung durch Skalierung bzw. Verkleinerung der zentralen MOSFET Bauelemente in komplementären integrierten Schaltkreisen - auch bekannt unter der Mooreschen Gesetzmäßigkeit. In naher Zukunft werden sich die kleinsten Strukturgrößen dieser Bauelemente atomaren Dimensionen annähren. Aufgrund der damit steigenden Komplexiät der Herstellung, verlangsamt sich dieser Skalierungstrend und kommt unter Umständen im Bereich von sub-10nm Technologieknoten vollständig zum Erliegen.

Aus diesem Grund sind neue Technologien, welche zukünftig potential die CMOS Technologie ersetzen könnten, ein Forschungsschwerpunkt von Wissenschaft und Industrie. Auf Basis existierender Halbleiterfertigungsprozesse bieten hierzu neuartige Bauelemente mit speziellen Charakteristiken vielversprechende Lösungen, um innovative Schaltungsarchitekturen in nanoskaligen integrierten Logikschaltungen zu ermöglichen. Ein Anwärter aus diesem Forschungsbereich sind polarititätskontrollierbare bzw. rekonfigurierbare MOSFET (RFET) Konzepte. Diese RFET Bauelemente können, im Gegensatz zu herkömmlichen MOSFETs, mit Hilfe eines elektrischen Signals zwischen n- und p-Typ Leitungsmechanismus umgeschaltet werden. Diese Wahlmöglichkeit verspricht, komplexere Systeme mit geringer Bauelementanzahl und geringeren Kosten pro logischer Funktion herzustellen.

Der Fokus dieser Arbeit liegt sowohl auf der Demonstration des erfolgreichen Transfers einer Silizium Nanodraht RFET Vorläufertechnologie in eine planare RFET Bauelementarchitektur als auch der parallelen Optimierung dieser für rekonfigurierbare sowie konventionelle CMOS Schaltungen.

Analog zu den vorausgegangenen Nanodraht RFET zeichnet sich der planare Ansatz durch einen dotierstofffreien CMOS kompatiblen Herstellungsprozess auf Basis eines konventionellen SOI Substrates aus und erlangt seine Rekonfigurierbarkeit durch elektrostatische Dotierung. Das planare Bauelement kann als eine Verknüpfung von zwei MOSFETs in einer gemeinsamen Struktur betrachtet werden. Diese Transistorstruktur besteht aus einem mittig oberseitigen Verarmungstyp FET, der auf einen rückseitigen Schottky Barriere Anreicherungstyp FET (SBFET) aufbaut. Der rückseitige SBFET etabliert dabei wahlweise den leitfähigen n- oder p-Kanal durch ein entsprechend angelegtes elektrisches Potential auf dessen Gate-Elektrode. Die eigentliche Kontrolle des Ladungsträgerflusses zwischen Quelle und

Senke wird durch den oberseitigen FET mittels einer lokalen Verarmung des rückseitigen Kanals über ein gegensätzliches Potential auf der oberseitigen Gate-Elektrode realisiert.

Zwei Generationen planarer RFET Bauelemente wurden erfolgreich prozessiert. Dabei wurden verschiedene Gate-Elektrodenmaterialien, wie beispielsweise Nickel, Aluminium und reaktiv kathodenzerstäubtes Wolfram-Titan-Nitrid untersucht. So konnte unter anderem experimentell Wolfram-Titan-Nitrid als geeignet für die Realisierung einer symmetrischen n- und p-Typ Schaltcharakteristik des selben Bauelements, als essentielle Voraussetzung für RFET Schaltungsdesigns, identifiziert werden. Des Weiteren wird ein experimentelles Verfahren zur Einstellung der Schottky Barrierehöhe für eine ideale n- und p-Typ Leitungssymmetrie, welches auf einer Dotierstoffsegration mittels Silizidierung basiert, demonstriert.

Umfassende elektrische Charaktiersierungsergebnisse zeigen experimentelle Unterschwellensteigungen von 65 mV/dec und an-zu-aus Stromverhältnisse von über 9 Dekaden. Auf Basis von kalibrierten TCAD Simulationen wird der Designraum dieses Bauelementekonzeptes untersucht, um Prognosen für skalierte und zusätzlich optimierte Bauelemente abzuleiten. Ebenfalls wird die Hochtemperaturleistungsfähigkeit evaluiert und sowohl mit der Nanodraht RFET Vorgängertechnologie als auch mit dem industriellen Stand der Technik an Hochzuverlässigkeits und -temperatur MOSFETs verglichen. Dieser Vergleich zeigt deutlich die gleichwertige Leistungsfähigkeit der planaren RFET Technologie hinsichtlich des Leckstromniveaus im Aus-Zustand.

Abstract

In the last 50 years, our economy and society have obviously been influenced and shaped to a great extent by electronic devices. This substantial impact of electronics is the result of a continuous performance improvement based on the scaling, i.e. shrinking, of MOSFET devices in complementary integrated circuits, following Moore's law. As the MOSFET feature sizes are approaching atomistic dimensions, the scaling trend slowed down considerably and is even threatened for sub-10 nm technology nodes. Therefore, technologies that have the potential to supersede the CMOS technology in the future are the topic of intensive investigation by both researchers and the industry. An attractive solution is the leveraging of existing semiconductor technologies based on emerging research devices (ERD) offering novel characteristics, which enable new circuit architectures in future nanoscale logic circuits. A possible ERD contender are polarity controllable or reconfigurable MOSFET (RFET) concepts. Generally, RFET devices are able to switch between n- and p-type conduction by the application of an electrical signal. Therefore, RFET promise increased complex systems with a lower device count decreasing the costs per basic logic function based on their higher logic expressiveness.

The focus of this work lies in the successful transfer of a predecessor silicon nanowire (NW) RFET technology into a planar RFET device, while simultaneously optimizing the resulting RFET for reconfigurable as well as conventional CMOS circuits. As for the predecessor NW RFET, the planar approach features a doping-less CMOS compatible fabrication process on a conventional SOI substrate and obtains its reconfigurability by electrostatic doping. The device can be regarded as a entanglement of two MOSFET in one structure, i.e. a depletion mode FET centered on top of a backside enhancement mode Schottky barrier FET (SBFET). The backside SBFET establishes the conductive channel consisting of the desired charge carrier type via an appropriate potential on its gate electrode. The topside FET controls the charge carrier flow between source and drain by locally depleting this channel given an opposite potential on its gate electrode with respect to the backside gate electrode.

Two generations of devices have been successfully processed, while different gate electrode materials, i.e. nickel, aluminum and reactively sputtered tungsten-titanium-nitride, have been introduced to the device structure. As n- and p-type symmetry of the very same device is essential for RFET circuit design, tungsten-titanium-nitride is experimentally identified as a possible mid-gap metal gate electrode for RFET devices. Also, a Schottky barrier adjustment process for ideal n- and p-type symmetry based on silicide induced dopant segregation is experimentally demonstrated.

Extensive electrical characterizations supported by calibrated TCAD simulations are presented, demonstrating experimental sub-threshold slopes of 65 mV/dec and on-to-off current ratios of over 9 decades. Based on TCAD simulations and supported by experimental results, the design space of the device concept is explored in order to gather predictive results for future scaled device optimization. Further, the high temperature (HT) performance is evaluated and compared to the predecessor NW RFET devices as well as to a state-of-the-art industrial high reliability HT MOSFET clearly illustrating the on par performance of the planar RFET concept with respect to off-state leakage current.

Contents

1 Introduction

In the last 50 years, our economy and society have obviously been influenced and shaped to a great extent by electronic devices. This substantial impact of electronics is the result of a continuous performance improvement of the central driving element of modern electronics, the metal-oxide-semiconductor field-effect transistor (MOSFET). The increase in performance mainly stems from the scaling, i.e. shrinking, of the MOSFET devices in complementary integrated circuits (CMOS). This continuous scaling trend has already been predicted in 1968 by G. E. Moore later being referenced to as Moore's law. The main benefits of scaling are threefold. Firstly, scaling results in a lower cost per transistor as more devices are crammed into the same silicon area. Also, the MOSFET becomes faster as charge carriers travel over a smaller distance and the associated capacitance, which has to be charged and discharged, is reduced. Finally, the decreasing capacitance together with voltage scaling results in a higher energy efficiency of CMOS circuits [1].

Today, as the MOSFET feature sizes are approaching atomistic dimensions as the hard physical limit, the scaling trend slowed down considerably and is even threatened for sub-10 nm technology nodes. Besides increasing short channel effects and ultimately direct S/D tunneling, mainly the power density and dissipation slowed down the pace of CMOS scaling. Further, additional advancements are increasingly difficult to realize both from the technological and especially the economical perspective. As the demand for increased electronic device and system performance is tremendous, the industry is seeking ways to continue scaling summarized by the International Technology Roadmap for Semiconductors group (ITRS 2.0) in the focus team "More Moore", which concentrates efforts across interdisciplinary technology work groups. However, it is generally expected, that Moore's law is going to end within the next decade due to economical reasons [2]. Therefore, technologies that have the potential to supersede the CMOS technology in the future are the topic of intensive investigation by both researchers and the industry. These efforts result in emerging research devices (ERD) that are continuously reviewed by the ITRS 2.0 "Beyond CMOS" focus team. Many ERD approaches are under investigation, e.g. new disruptive materials like carbon nanotubes, graphene and other 2D materials. Also, completely different information representation schemes, e.g. quantum computing, spintronics and memristor based logic, are evaluated. However, all these approaches have to be regarded as still being in their infancy stages.

For this reason, the leveraging of existing semiconductor technologies based on ERD offering novel characteristics, which enable new circuit architectures in future nanoscale logic circuits,

is considered as a promising approach for "Beyond CMOS". These novel characteristics must be able to enhance the functionality of electronic systems in order to serve the high market demand for increasing performance and system complexity.

A possible "Beyond CMOS" contender of ERD are polarity controllable or reconfigurable MOSFET (RFET) concepts. Generally, RFET devices are able to switch between n- and p-type conduction via electrostatic doping (ED) by applying an appropriate electrical signal. Lately, ED has increasingly attracted research interest [3–8], while one of the first demonstrations of electrostatically doped RFET have been reported by Koo et al. [9] followed by Colli et al. [10] and Wessely et al. [11, 12]. Generally, the RFET concepts promise increased complex systems with a lower device count mitigating the power density issue and decreasing the costs per basic logic function based on their higher logic expressiveness [13, 14]. Additionally, the concepts require only minimal modifications or even simplifications of standard technology process flows [14]. It has to be noted, that the majority of RFET research is focused on extending end-of-roadmap nanowire and gate-all-around FET structures, while the work presented here considers the less ambitious possibility of leveraging the economically successful and matured planar FDSOI technology [15].

The focus of this work lies in a technology transfer of the nanowire (NW) RFET ERD of Wessely et al. [16] into a planar RFET device structure. Simultaneously, an optimization of the planar device performance for reconfigurable as well as conventional CMOS circuit application and a reduction of the technological complexity are targeted. As for the predecessor NW RFET, the planar approach features a doping-less CMOS compatible fabrication process on a conventional SOI substrate and obtains its reconfigurability by electrostatic doping. The device can be regarded as a entanglement of two MOSFET in one structure, i.e. a depletion mode FET centered on top of a backside enhancement mode Schottky barrier FET (SBFET). The backside SBFET establishes the conductive channel consisting of the desired charge carrier type via an appropriate potential on its gate electrode. The topside FET controls the charge carrier flow between source and drain by locally depleting this channel given an opposite potential on its gate electrode with respect to the backside gate electrode.

Two generations of planar RFET devices have been successfully processed, while different gate electrode materials, i.e. nickel, aluminum and reactively sputtered tungsten-titanium-nitride, have been introduced to the device structure. As n- and p-type symmetry of the very same device is essential for RFET circuit design, a capable Schottky barrier tuning process based on silicide induced dopant segregation is experimentally demonstrated.

Extensive electrical characterizations supported by calibrated TCAD simulations are presented, demonstrating experimental sub-threshold slope of 65 mV/dec and on-to-off current ratios of over 9 decades. Based on TCAD simulations and supported by experimental results, the design space of the device concept is explored in order to gather predictive results for fu-

ture scaled device optimization. Further, the high temperature (HT) performance is evaluated and compared to the predecessor NW RFET devices as well as to a state-of-the-art industrial high reliability HT MOSFET clearly illustrating the on par performance of the planar RFET concept with respect to off-state leakage current.

This thesis is structured as follows. In the first part, the basic theoretical foundation of MOSFET and Schottky barrier physics and their fabrication technology as well as an overview on electrostatically doped RFET concepts are presented. Thereafter, experimental results and TCAD simulations of long-channel as well as simulatively scaled RFET devices are discussed. Next, the experimental high temperature characteristics and simulatively predicted device performance for up to 550 K are illustrated. Finally, as part of an outlook, an optimized planar RFET device with remarkable superior characteristics is simulatively proposed for future RFET research.

2 Theoretical Considerations

In this chapter, an introduction is given to the most important principles, device concepts and parameters of metal-oxide-semiconductor field-effect transistors (MOSFET). Before introducing the working principles of MOSFET devices it is insightful to discuss the central building block of field-effect transistors (FET), the metal-oxide-semiconductor capacitor (MOSCAP). Thereafter, the fundamentals of charge carrier injection of Schottky barriers (SB) formed by a metal-to-silicon contact are presented followed by the actual introduction of MOSFET device concepts and their relevant DC-parameters. Finally, this chapter closes with an overview of today's reconfigurable FET (RFET) device concepts.

2.1 The Metal-Oxide-Semiconductor Capacitor (MOSCAP)

Fig. 1 illustrates a cross-section of an idealized[a] MOSCAP structure and its corresponding energy band diagram for the case of a p-type semiconductor in thermal equilibrium. For simplification, the work functions of the semiconductor (ϕ_S) and the metal (ϕ_M) are defined to be identical, resulting in a flat conduction (E_C) and valence band (E_V), known as flat-band[b] condition, for:

$$V_G = 0 = \phi_M - (\chi_S + \frac{E_G}{2q} + \psi_B)$$

where V_G is the applied voltage to the top side electrode of the MOSCAP, χ_S the electron affinity of the semiconductor, E_G the band gap and ψ_B the bulk Fermi potential ($\psi_B = E_i - E_{FS}$).

By applying an external voltage V_G, a surface potential ψ_{SF} builds up at the semiconductor-oxide interface (Fig. 2). The potential changes the charge carrier distribution near the semiconductor surface. This physical effect is the corner stone for the transistor effect in field-effect based semiconductor devices, i.e. the MOSFET. Depending on the magnitude of ψ_{SF}, three cases of charge carrier redistribution can be distinguished for the idealized MOSCAP [17, pp.160].

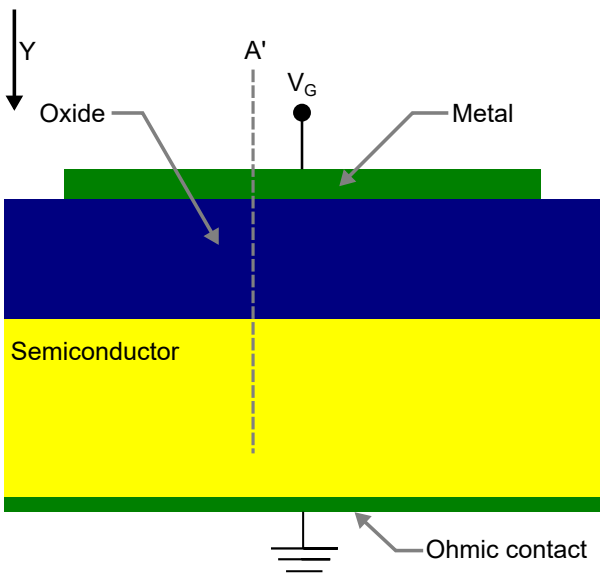
Given a p-type[c] semiconductor, applying a negative voltage ($V_G < 0V$) results in $\psi_{SF} < 0V$ and an upward bending of the bands close to the surface. Consequently, positive excess majority charge carriers, i.e. holes, are attracted to the surface (Fig. 2a). This state is called *accumulation* and the surface hole concentration $p_{p,SF}$ is given by:

$$p_{p,SF} = n_i e^{q(\psi_B - \psi_{SF})/k_B T}$$

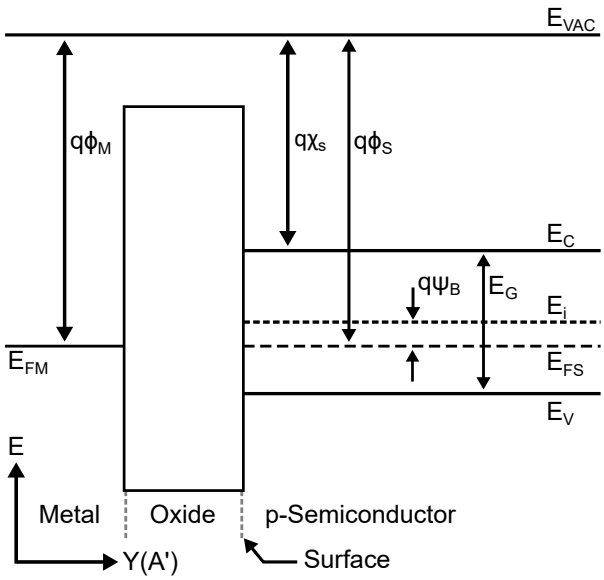
[a] Ideal infinite oxide resistivity, identical metal and semiconductor work function ϕ_M=ϕ_S and charges only exist in the semiconductor and the metal electrode with opposite signs.

[b] In the non-ideal case, a voltage $V_G = V_{FB}$ has to be applied to establish the flat-band condition.

[c] For an n-type semiconductor, replace $q\psi_B$ by $-q\psi_B$.



(a) Schematic Cross-section of a MOS capacitor structure.



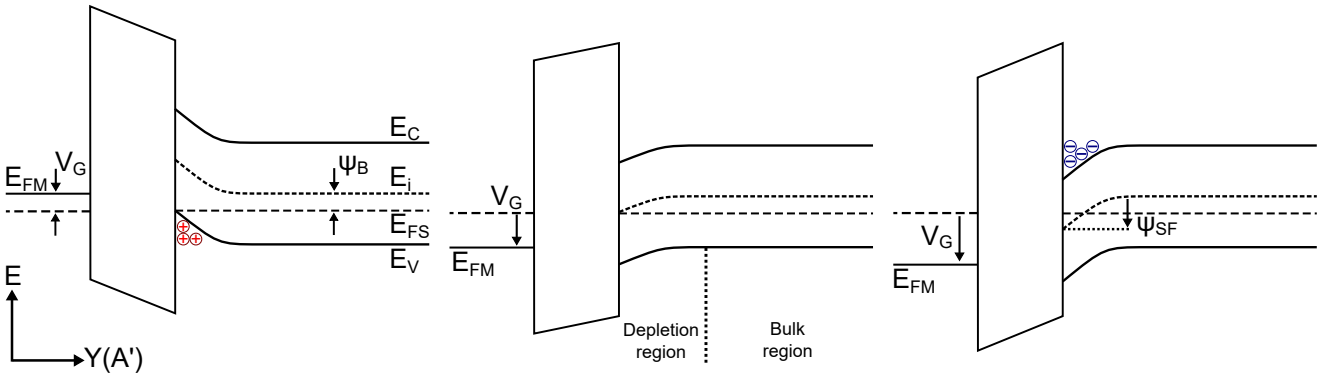
(b) Schematic energy band diagram of an idealized MOS capacitor based on a p-type semiconductor in flat-band condition.

Fig. 1: Ideal MOSCAP structure and corresponding energy band diagram.
ϕ_M, ϕ_S work function of metal and semiconductor; χ_S electron affinity of the semiconductor; ψ_B bulk Fermi potential; E_G band gap; E_C bottom edge of the conduction band; E_i intrinsic Fermi level; E_{FM}, E_{FS} Fermi level of the metal and the semiconductor; E_V top edge of the valence band; q elementary charge.

On the other hand, when a sufficiently small positive voltage ($V_G > 0V$) is applied, ψ_{SF} rises and the energy bands begin to bend downwards. This leads to a repelling of holes from the surface leaving behind negatively ionized acceptor dopant atoms in the lattice. This is called *depletion* condition and is defined by $\psi_B > \psi_{SF} > 0V$ for the idealized case. An increase of the positive voltage bends the bands further to a point, where the intrinsic Fermi Level E_i crosses over the Fermi level E_{FS} at the surface, i.e. $\psi_{SF} = \psi_B$, as shown in Fig. 2b. This condition marks the onset of *weak inversion*, where the applied voltage starts to induce negative excess minority charge carriers, i.e. electrons, as a thin layer at the surface. The *weak inversion* regime is defined by $2\psi_B > \psi_{SF} > \psi_B$. The electron surface concentration $n_{p,SF}$ is given by:

$$n_{p,SF} = n_i e^{q(\psi_{SF} - \psi_B)/k_B T}$$

The onset of the so called *strong inversion* condition is defined by $\psi_{SF} = 2\psi_B$ where the minority carrier concentration near the surface equals the bulk majority concentration (Fig. 2c). Further increases of ψ_{SF} result in an additional increase of the $n_{p,SF}$ charge concentration, which is used as the controllable conductive element, i.e. the *channel*, in MOSFET devices as described later [18, pp.228].



(a) Accumulation of majority charge carriers (holes) at the insulator-semiconductor interface ($\psi_{SF} < 0\ V$).

(b) Depletion $\psi_B > \psi_{SF} > 0V$ and onset of weak inversion ($\psi_{SF} \geq \psi_B$), i.e. onset of attraction of minority charge carriers (electrons).

(c) Onset of strong inversion ($\psi_{SF} = 2\psi_B$), i.e. surface concentration of minority charge carriers equals bulk majority carrier concentration.

Fig. 2: Schematic energy band diagrams of the MOSCAP on p-type substrate for different biasing conditions. Elementary charge q omitted for clarity.

2.2 The Metal-to-Silicon Contact

In this chapter, an overview of the physical mechanisms of the electrical transport as well as technological aspects for the realization and manipulation of Schottky barrier (SB) contact properties is presented. This technical background is mandatory for an understanding of the later described SBFET and RFET devices, where a SB at the source is responsible for the charge carrier injection. Besides the ideal SB contact, extended models and non-ideal deviations are briefly discussed, e.g. Schottky barrier lowering and Fermi level pinning. Focus is laid on nickel silicide (Ni_xSi_y) SB technologies as these are essential to the later presented RFET devices.

2.2.1 Fundamentals of Schottky Barrier Physics

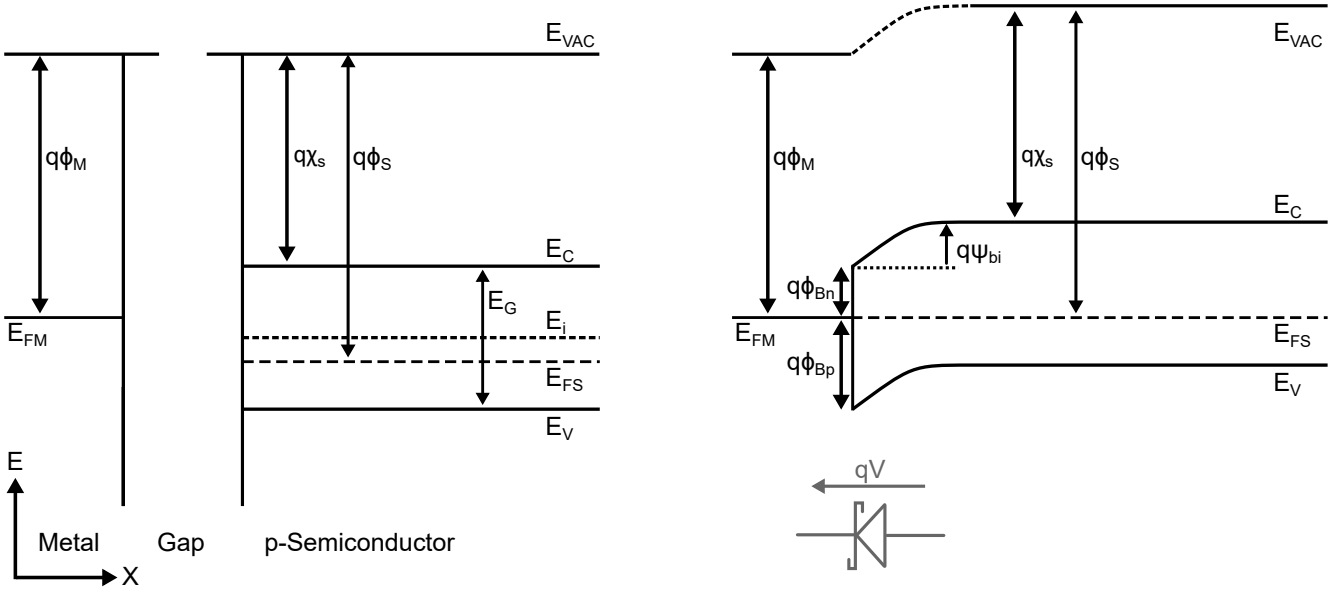
The metal-to-semiconductor contact, also know as Schottky contact, is a complex physical phenomenon exhibiting either a rectifying or ohmic behavior depending on the physical properties of the metal and the semiconductor as well as their combination.

Fig. 3 illustrates the effect on the idealized energy bands before and after the theoretical joining of a moderately doped p-type semiconductor with a metal in thermal equilibrium. Combining a p-type semiconductor with a work function ϕ_S with a metal with a work function $\phi_M < \phi_S$ results in the alignment of the Fermi level and consequently the formation of an abrupt discontinuity or barrier at the interface for both electrons and holes, known as the Schottky barrier.

For the formation of a SB contact on an n-type semiconductor, the relations are inverted [17, pp.229], [19, pp.134].

The barrier height for holes ϕ_{Bp} and electrons ϕ_{Bn} in the case of an ideal SB contact is linearly linked to the electron affinity of the semiconductor χ_{S} and the metal work function ϕ_{M} by:

$$q\phi_{\mathrm{Bp}} = E_{\mathrm{G}} - q\phi_{\mathrm{Bn}} \quad \text{with} \quad \phi_{\mathrm{Bn}} = \phi_{\mathrm{M}} - \chi_{\mathrm{S}} \quad \text{and} \quad E_{\mathrm{G}} = q\left(\phi_{\mathrm{Bp}} + \phi_{\mathrm{Bn}}\right)$$



(a) Separated band diagrams of metal and p-type semiconductor

(b) Band diagram after joining and forming a SB contact and corresponding Schottky diode symbol.

Fig. 3: Schematic band diagram of an ideal SB contact in thermal equilibrium a) before and b) after theoretically joining a metal with a p-type semiconductor for $\phi_{\mathrm{M}} < \phi_{\mathrm{S}}$.
ϕ_{M}, ϕ_{S} work function of metal and semiconductor; χ_{S} electron affinity of the semiconductor; E_{G} band gap; E_{Vac} vacuum energy level; E_{C} bottom edge of the conduction band; E_{i} intrinsic Fermi level; E_{FM}, E_{FS} Fermi level of the metal and the semiconductor; E_{V} top edge of the valence band; ϕ_{Bp}, ϕ_{Bn} potential barrier for holes and electrons; ψ_{bi} build in potential; q elementary charge.

By applying a sufficiently negative potential ($V = +V_F$) to the metallic side of the contact the build in potential ψ_{bi} is reduced and majority charge carriers, i.e. holes, are able to drift and diffuse out of the semiconductor into the metal.[a] This biasing condition is referred to as the forward biasing of the SB by $+V_F$. In the opposite case, applying a positive potential to the

[a] As holes are quasi-particles, electrons are actually injected from the metal into the valence band of the p-type semiconductor annihilating holes.

metal ($V = -V_R$) increases ψ_{bi} and inhibits the hole transport. This biasing condition is referred to as reverse biasing of the SB by $-V_R$. The unbiased build in potential ψ_{bi} can be derived from:

$$\psi_{\mathrm{bi}} = \phi_{\mathrm{Bn}} - \frac{E_{\mathrm{C}} - E_{\mathrm{FS}}}{q} = \phi_{\mathrm{M}} - \phi_{\mathrm{S}}$$

The region of band bending, where the charge concentration is modified in relation to the bulk concentration, is called the depletion or the space-charge region. The width of the space-charge region W_{SCR} for a constant doping concentration is given by [19, pp.136] (Fig. 4):

$$W_{\mathrm{SCR}} = \sqrt{\frac{2\kappa_{\mathrm{S}}\epsilon_0}{qN_{\mathrm{A/D}}}\left(\psi_{\mathrm{bi}} - V - \frac{k_{\mathrm{B}}T}{q}\right)}$$

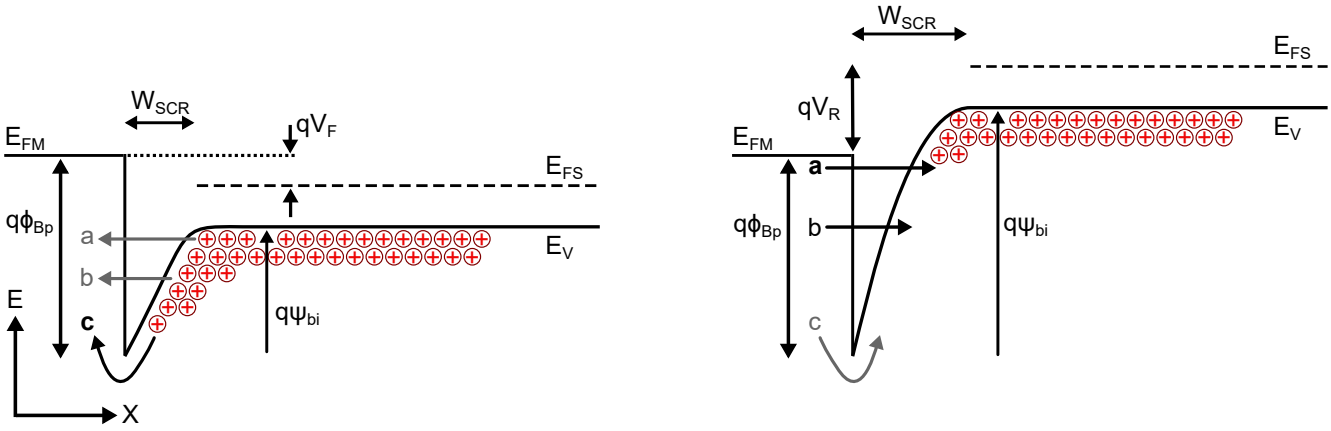
where κ_{S} is the permittivity of the semiconductor, $N_{\mathrm{A/D}}$ the constant acceptor or donor doping concentration, V the applied potential ($+V_F$ or $-V_R$) and $k_{\mathrm{B}}T/q$ the thermal voltage.

Charge carriers can pass the SB from and into the metal by five distinct transport mechanisms [19, pp.153].

(a) direct quantum-mechanical tunneling or field emission through the barrier (FE)
(b) thermionic field emission through the barrier at an elevated energy level (TFE)
(c) thermionic emission over the top of the barrier (TE)
(d) recombination inside the depletion zone
(e) diffusion of minority carriers

For SB at room temperature on moderately doped semiconductors ($N_{\mathrm{A/D}} < 10^{17} cm^{-3}$), the dominant transport process into or from the metal is either FE, TFE or TE (Fig. 4). The charge carrier transport based on FE requires a sufficiently thin SB in the order of a few nanometers of tunneling distance at or below the Fermi level. In case of thermionic field emission, charge carriers acquire thermal energy prior a tunneling process. The thermal stimulation raises the charge carrier to an energy level above the Fermi energy where a sufficiently thin barrier is located. The mechanism of thermionic emission is based solely on thermal stimulation of charge carriers over the top of the barrier.

For forward biasing and a resulting reduction of ψ_{bi}, thermionic emission is dominating the total charge carrier transport (Fig. 4a). At room temperature and under reverse biasing conditions, i.e. increased ψ_{bi}, thermionic field emission is mainly contributing to the charge carrier transport, while under strong reverse biasing condition leading to increased band bending and barrier thinning field emission starts to become dominant (Fig. 4b).



(a) SB under forward biasing

(b) SB under strong reverse biasing

Fig. 4: Schematic band diagram of a SB contact for forward and reverse biasing condition. a) FE, b) TFE and c) TE.

For increased dopant concentrations up to degenerated levels at the SB and decreasing temperatures, the relative contribution of FE to the total current increases as high doping levels reduce the space charge region width (W_{SCR}) and TE and TFE exhibit a more pronounced temperature dependence than FE [19, p.166]. Also, degenerated levels of doping concentration result in biasing-independent contact properties and are commonly used to fabricated Ohmic interconnects in semiconductors.

An estimation of the dominant transport mechanism depending on doping concentration and temperature can be derived by comparing the following transport energy factor Z with the thermal energy $k_{\mathrm{B}}T$ [19, pp.165]:

$$Z = \frac{q\hbar}{2} \cdot \sqrt{\frac{N_{\mathrm{A/D}}}{m^* m_0 \cdot \kappa_{\mathrm{S}} \epsilon_0}}$$

For the case of $k_{\mathrm{B}}T \ll Z$ field emission is the driving transport mechanism. Vice versa, for $k_{\mathrm{B}}T \gg Z$ TE is dominant. For $k_{\mathrm{B}}T \approx Z$ the combined transport via TFE is the main current transport process.

The current density contribution of TE (J_{TE}) over a SB is given by the general expression [20–22]:

$$J_{\mathrm{TE}} = A^{**} T^2 \exp\left(-\frac{q\phi_{\mathrm{B}} - q\Delta\phi}{k_{\mathrm{B}}T} \right) \left[\exp\left(\frac{qV_{\mathrm{A}}}{k_{\mathrm{B}}T} \right) - 1 \right]$$

where A^{**} is the effective Richardson constant, T the temperature, $\Delta\phi$ the barrier lowering contribution (as described below) and V_A the voltage applied to the SB.

A generally accepted approximation of the tunneling probabilities $T_{n,p}$ for electrons and holes is based on the Wentzel-Kramers-Brillouin (WKB) approximation of a triangular energy barrier using the respective effective carrier mass m^* as a fitting parameter [23, pp.741],[20–22]:

$$T_{n,p} \propto \exp\left(\frac{4 \cdot \sqrt{2m^* m_0} \cdot {\phi_B}^{3/2}}{3q\hbar\mathscr{E}_x}\right)$$

where $\mathscr{E}_x$ is the electrical field across the SB.

Based on $T_{n,p}$ the FE current density contribution J_{FE} through the SB can be obtained by the transport model of Schenk and Heiser [21, 22, 24]:

$$J_{FE} = \frac{qm^* k_B T}{2\pi^2\hbar^3} \int_{q\phi_{Bp}}^{q\phi_{Bn}} dE \cdot T_{n,p} \times \ln\left[\frac{1+\exp(E-E_{FS})/k_B T}{1+\exp(E-E_{FM})/k_B T}\right]$$

In the presence of an perpendicular electric field ($\mathscr{E}_x$) at the SB interface, i.e. $\mathscr{E}_x$ either applied externally or caused by the build in potential ψ_{bi}, the SB height is lowered, known as the Schottky effect or Schottky barrier lowering (SBL) (Fig. 5) [19, pp.146], [18, pp.143],[21, 25]. This lowering is induced by the image-force effect, that arises when an electron approaches a perfect conductor (metal) and induces a positive charge of the same magnitude in the conductor resulting in an attractive force between both charges. The positive charge in the metal is referred to as the image charge. The magnitude of barrier lowering $\Delta\phi$ is given by [19, p.148]:

$$\Delta\phi = \sqrt{\frac{q|\mathscr{E}_x|}{4\pi\kappa_S\epsilon_0}}$$

Fig. 5 illustrates the SBL effect for a p-type semiconductor in equilibrium and under forward as well as reverse biasing conditions. The lowest barrier height is obtained for reverse biasing, as the electric field increases for this condition, while for forward biasing the barrier is slightly higher than in the case of thermal equilibrium. In essence, the barrier height becomes bias dependent.

Contrary to the formation of Ohmic SB contacts on degenerately doped semiconductors, a well controlled and reproducible rectifying SB contact is far from being trivial to accomplish. Merely placing metal layers on top of semiconductor surfaces constantly does not result in the formation of an ideal SB contact in the sense of the Schottky-Mott relation [26, 27]. This

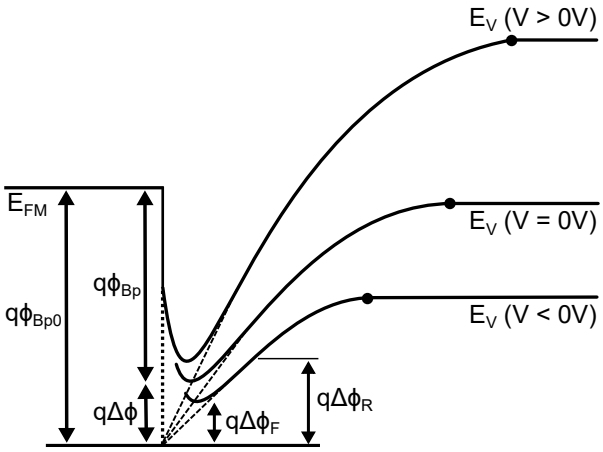


Fig. 5: Band diagram with SBL for a p-type semiconductor under forward, equilibrium and reverse biasing. ϕ_{Bp0} intrinsic barrier height for holes; ϕ_{Bp} barrier height for holes in thermal equilibrium ($V = 0$); $\Delta\phi_{\mathrm{R}}$, $\Delta\phi_{\mathrm{F}}$ barrier lowerings under reverse and forward bias, respectively. Derived from [19, p.149].

is mainly attributed to metal-induced interface states, crystal lattice irregularities or interdiffusion and defects as well as surface contamination [19, pp.139],[27]. The non-ideal interface states alter the effective SB height and fix the Fermi potential on the surface limiting the effect of the metal work function. This effect is described in the literature as Fermi level pinning [28], [19, pp.144], [18, pp.146]. Besides Fermi level pinning, surface dipoles and differences in electronegativity additionally alter the height of the SB. Surface dipoles can be induced by crystal defects and dopants or other impurity atoms at the interface [28] but also have been predicted and modeled for atomically clean and abrupt interfaces [29–33]. A recent in depth overview of these complicated phenomena is given by R. Tung in [27].

One possibility to mitigate the described surface related issues of SB formation on silicon, is the implementation of technologies based on chemical reactions between metal and the underlying silicon, i.e. silicidation processes. Silicidation results in buried and therefore less contaminated SB interfaces and has been extensively studied in the context of barrier-height engineering. A brief overview of technological aspects of silicidation technologies is presented in the following section.

2.2.2 Technological Aspects of Silicide Schottky Barrier Engineering

Silicide technologies have been studied for over 50 years and have been introduced in the semiconductor industry in the 1980s as a substitute or support for the heavily doped polysilicon used as contact metalization and local wiring [34]. This development is based on the advantageous properties of many silicides as they fulfill the basic requirements of low specific and contact resistivity, high thermal stability and good processibility as well as process compatibility with standard Si-based CMOS technologies [35]. Today, silicides are commonly

used as Schottky and Ohmic contacts as well as interconnects and the self-aligned silicidation process, known as salicide process, is a corner stone technology for high-performance CMOS applications.

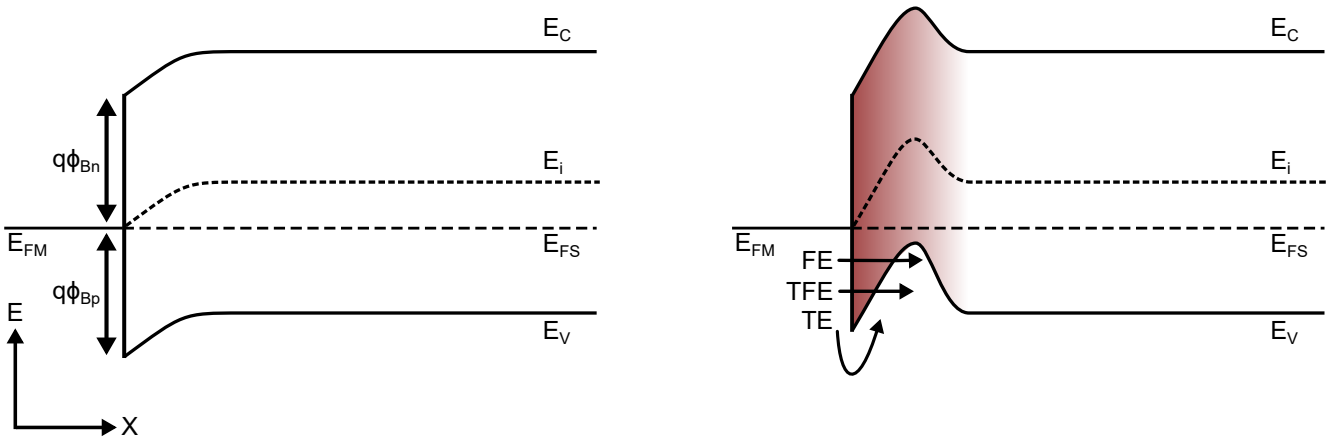
The conducted research on altering the silicide properties covers, amongst others, the use of different metallic elements and composites for the silicidation process, pre-/post-silicidation ion implantation and diffusion doping, silicidation temperature profiles and dopant segregation mechanisms. Here, focus is layed on dopant segregation mechanisms for the effective Schottky barrier height (eSBH) tuning.
Various processes have been demonstrated to alter the effective Schottky barrier height (eSBH) holes and electrons respectively, and to increase the thermal stability of silicides. Most of this research is focused on nickel silicide (NiSi), which replaced $TiSi_2$ and $CoSi_2$ in the semiconductor industry in the past decade. It is noteworthy, that the silicidation mechanisms and properties differ with respect to the geometric confinement during silicidation as it is the case for 2D or nanowire contacts in comparison to bulk and conventional thin film substrates [36]. Especially, deeply scaled nanowire and FinFET structures are prone to low yield due to overly tight process windows and thermal budget limitations as described in [36–38].

In order to fabricate Schottky barrier MOSFET (SBFET) devices with on par performance compared to conventionally doped MOSFET, it is necessary to reduce the parasitic SB junction resistance by decreasing the effective barrier height well below 100 meV what is more complicated to achieve for n-type barriers than for p-type [31, 32, 39]. Different groups have demonstrated low SB heights using NiSi and different ion implantation schemes [40–42]. A sulfur ion implant followed by a drive-in anneal for the segregation of sulfur at the NiSi/Si interface has successfully resulted in eSBH of <10 meV for gate-first high-κ/metal-gate NMOS [40, 43]. Similarly, PMOS with 12 meV based on aluminum segregation have been reported in [44]. Ultimately, Chen et al. present an Ohmic-like, virtually barrier free 0 eV eSBH for electrons with very low sheet resistance even on lightly doped Si using a Yb-ion implant prior to silicidation [42].

During silicidation of near-noble transition metals into doped silicon, dopants are redistributed along the silicide/silicon interface eventually forming a thin highly doped layer in the silicon. The first demonstration of dopant segregation was published by R. Thornten in 1981 using a thin p-doped interfacial layer to increase the PtSi Schottky barrier on n-type Silicon [45]. This mechanism is referred to as silicidation-induced dopant segregation (SIDS). This segregation occurs if three conditions are given:

- The solid solubility of dopants in the silicide must be low compared to Silicon [46].
- Point defects have to be present at the silicide/silicon interface [47].
- The intrinsic diffusion rate of the dopants in silicon has to be low at the silicdation temperature [46].

During SIDS, the dopants are expected to be snow-plowed by the growing silicide layer and being piled-up at the silicide/silicon interface as the silicide formation is consuming the silicon [46]. The snow-plowed dopants form a thin highly doped layer. A large fraction of these dopants is located at substitutional sites in the silicon lattice and is therefore electrically active [47]. As a consequence, these dopants cause a localized energy band bending close to the silicide interface leading to an increased tunneling probability of carriers through the effectively lowered Schottky barrier [31],[19, pp.150] (see Fig. 6). Further, investigations based on atomistic first principles calculations and experiments suggest that certain dopants, i.e. boron, located at substitutional sites in the silicon lattice at the silicide/silicon interface induce local interfacial dipoles. These dopant induced dipoles additionally reduce the SB height for majority carriers of the pile up layer and compensate Fermi level pinning interface states [31–33] . More detailed descriptions of the segregation mechanism are presented in [46] and [47] .



(a) Midgap silicide with symmetric eSBH for holes and electrons

(b) Band bending induced by segregated p-type dopants and SBL

Fig. 6: Schematic energy band diagrams of midgap silicide on p-type substrate with and without segregation.

Dopant segregated dopant profiles have been demonstrated to be extremely steep. Zhao et al. experimentally achieved gradients by ion implantation into $NiSi_2$ silicide followed by a SIDS process reaching 1.4 and 3.5 nm per decade for arsenide and boron concentration profiles, respectively [48]. Fig. 7 summarizes the literature on eSBH of fabricated silicided Schottky barrier contacts. Interestingly, the eSBH of NiSi can be tuned below 0.1 eV for holes as well as electrons [31, 32, 39, 49]. Urban et al. demonstrated NiSi SB contacts with eSBH well below 0.1 eV using boron or arsenic ion implantation followed by dopant segregation [39]. Lately, Sun et al. extended this method by combining a dual implantation of boron and aluminum with microwave annealing resulting in eSBH of 0.07 eV for holes [49]. Also, lower contact resistivity and higher thermal stability have been achieved by adding platinum or palladium to the NiSi phases [35, 50, 51]. Further, thermal stability of NiSi has been improved by implanting

fluorine, chlorine or nitrogen into NiSi [41, 52–54]. In the next section, a brief introduction to the technology and formation process of Ni_xSi_y is presented.

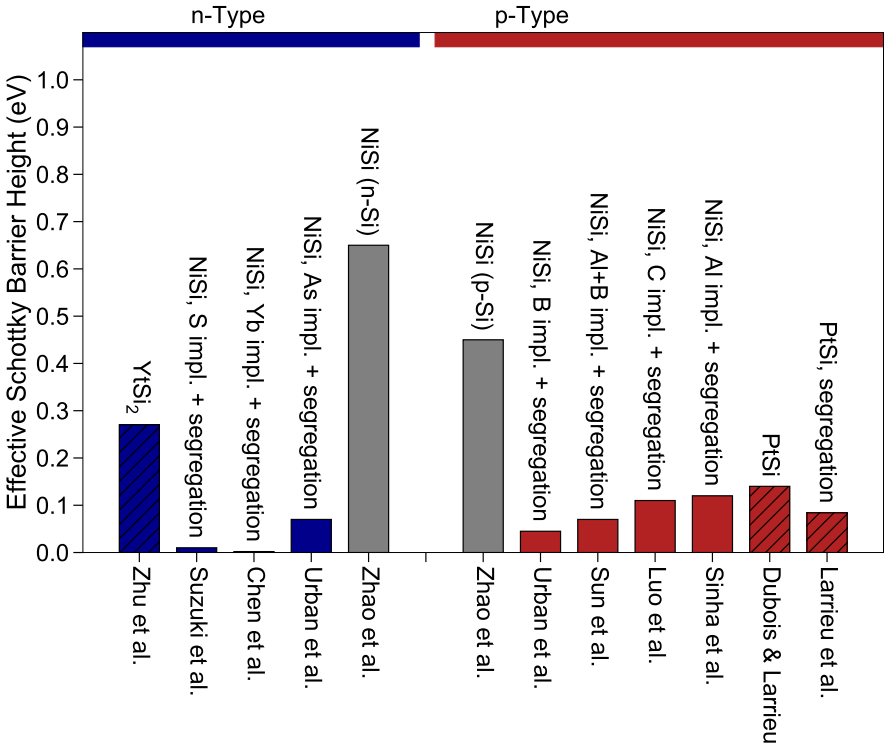


Fig. 7: Comparison of published effective SB heights.
Zhu et al. [55], Suzuki et al. [43], Chen et al. [42], Urban et al. [39, 56], Zhao et al. [40], Sun et al. [49], Luo et al. [57], Sinha et al. [44], Dubois & Larrieu [58], Larrieu et al. [59].

2.2.3 Nickel Silicide Technology

Compared to other silicides, e.g. $TiSi_2$ and $CoSi_2$, the transition metal silicide Ni_xSi_y offers many advantages especially for scaled nodes as low silicon consumption, low silicidation temperature, less mechanical stress and lower contact and sheet resistance [34, 36]. Further, rare earth silicides, e.g. $ErSi_2$ and $YbSi_2$, are known to be challenging to process while PtSi is relatively expensive [39, 50].

Ni_xSi_y features three ordered phases of interest, i.e. Ni_2Si, NiSi and $NiSi_2$ [35, 60]. The dominant phase is depending on the silicidation temperature as listed in Table 1. The most interesting phase for MOSFET fabrication is NiSi as it exhibits the lowest resistivity of 10-15 $\mu\Omega$cm [35].

In order to form a well controlled NiSi phase, a two step rapid thermal annealing RTA process is generally applied [34]. The RTA process provides a better annealing temperature and time control and reduces the risk of contamination compared to furnace annealing processes [35,

Phase	Formation Temp. (°C)	Resistivity ($\mu\Omega$cm)	Barrier height ϕ_{Bn} (eV)
Ni_2Si	200-325	25	
NiSi	350-600	10-20	0.64-0.67
$NiSi_2$	750-800	34	0.66

Tab. 1: Ni_xSi_y phases on bulk silicon [34, 35, 60–62].

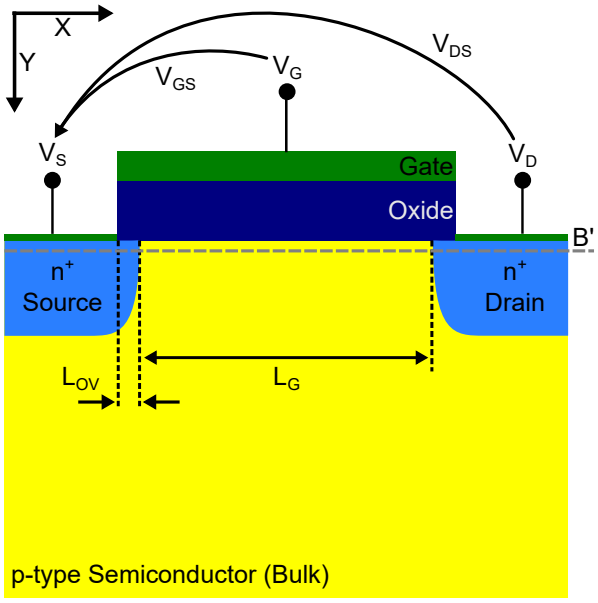
p.31]. At first, a soak annealing process step of $200 < T_1 < 325$ °C is applied to form the highly resistive metal-rich Ni_2Si phase. Afterwards, the excessive nickel is etched selectively, if it has not been fully consumed, and a second annealing process with $350 < T_2 < 600$ °C is applied to form the low resistance NiSi phase [61, 63].

2.3 Metal-Oxide-Semiconductor FET Concepts

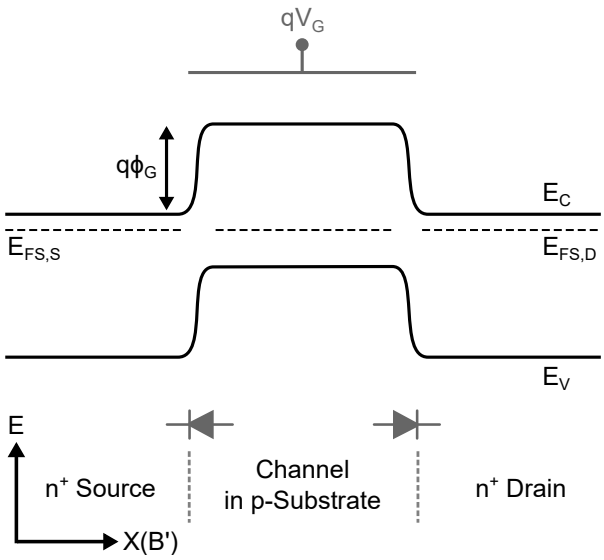
In this chapter, the fundamentals of long-channel metal-oxide-semiconductor field-effect transistors (MOSFET) are presented. Next, Schottky barrier FET (SBFET) devices are described as these represent the technical foundation for the afterwards following overview on electrostatically doped reconfigurable FET (RFET) concepts.

The classic MOSFET is a three terminal structure[a] based on a central MOS capacitor bordered by highly conductive contacts on opposite sides. Fig. 8a depicts an n-type MOSFET or NMOS integrated into a p-type semiconductor substrate. The conductive contacts are formed by heavily counterdoped n^+ regions, i.e. *source* and *drain*. Hence, source and drain (S/D) form back-to-back p-n junctions with the bulk semiconductor. Insulated by a thin oxide layer, the gate electrode is located between S/D overlapping both contact regions by L_{OV}. A charge carrier rich layer, i.e. the inversion layer or channel, below the oxide layer can be induced between S/D by the application of an appropriate gate potential V_G (see 2.1). This channel allows carriers injected at the source to flow to the drain, if a potential difference V_{DS} is applied between S/D. Note, that the gate overlap is mandatory for efficient charge carrier injection in conventional MOSFET devices. For NMOS (PMOS) devices, the source region injects electrons (holes) into the channel and is biased on the lowest (highest) potential accordingly [18, p.169]. By definition, all applied potentials are referenced to the source terminal voltage V_S, i.e. gate-source voltage V_{GS} and drain-source voltage V_{DS}. The bulk contact, a forth terminal not illustrated here, is commonly connected to the highest (for PMOS) or lowest (for NMOS) supply potential in CMOS circuits to avoid an undesired forward biasing of the S/D p-n junctions.

[a] Actually, a four terminal structure, if the bulk contact is included.



(a) Schematic Cross-section of an n-type metal-oxide-semiconductor field-effect transistor (MOSFET) structure.



(b) Schematic energy band diagram of an idealized NMOS based on a p-type semiconductor in thermal equilibrium.

Fig. 8: Schematic MOSFET structure and corresponding idealized energy band diagram. L_G gate length; L_{OV} gate overlap; V_G gate potential; V_S source potential; V_D drain potential; V_{GS} gate-source potential; V_{DS} drain-source potential; $E_{FS,S}$, $E_{FS,D}$ Fermi energy level at source and drain; E_C bottom edge of the conduction band; E_V top edge of the valence band; q elementary charge.

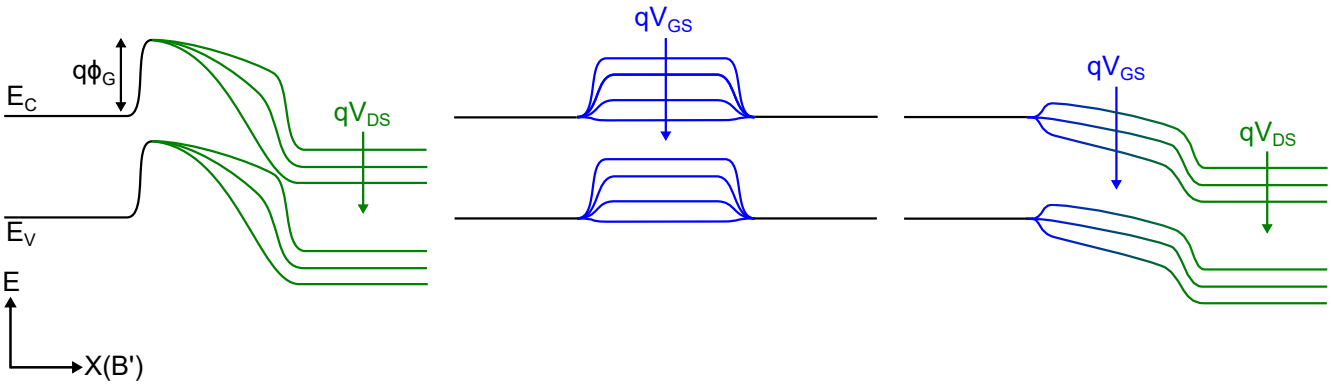
By applying a positive drain-source potential ($V_{DS} > 0\ V$), the Fermi energy of the drain region $E_{FS,D}$ is shifted downwards with respect to the Fermi energy of the source region $E_{FS,S}$ (Fig. 9a):

$$qV_{DS} = E_{FS,S} - E_{FS,D}$$

As the gate is not biased ($V_{GS} = 0\,V$), the electrons from the source are facing a potential barrier ϕ_G in the channel region inhibiting a charge carrier flow between S/D also referred to as transistor off-state.

On the other hand, biasing only the gate positively ($V_{GS} > 0\,V$, $V_{DS} = 0\,V$) results in a downward bending of the energy bands in the channel region and a reduction of ϕ_G and an increase of the surface potential ψ_{SF} (Fig. 9b). As described previously in chapter 2.1, the charge carriers are redistributed at the oxide-semiconductor interface depending on ψ_{SF}, i.e. for increasing ψ_{SF} from accumulation over flat-band to depletion, weak and finally strong inversion condition (Fig. 1b, Fig. 2). Therefore, only in weak and strong inversion condition a conductive channel is formed between source and drain.

Combining a sufficiently positive biasing of gate and drain ($V_{GS} > 0\,V$, $V_{DS} > 0\,V$) results in a current flow of excess electrons from the source through the established channel to the drain also referred to as transistor on-state (Fig. 9c). The gate-source voltage V_{GS} at which ψ_{SF} is sufficiently increased to enable the onset of a significant source-drain current is called threshold-voltage (V_{th}).



(a) Effect of V_{DS} for MOSFET in off-state $V_{GS} = 0\ V$

(b) Effect of V_{GS} for MOSFET in off-state $V_{GS} > 0\ V$, $V_{DS} = 0\ V$

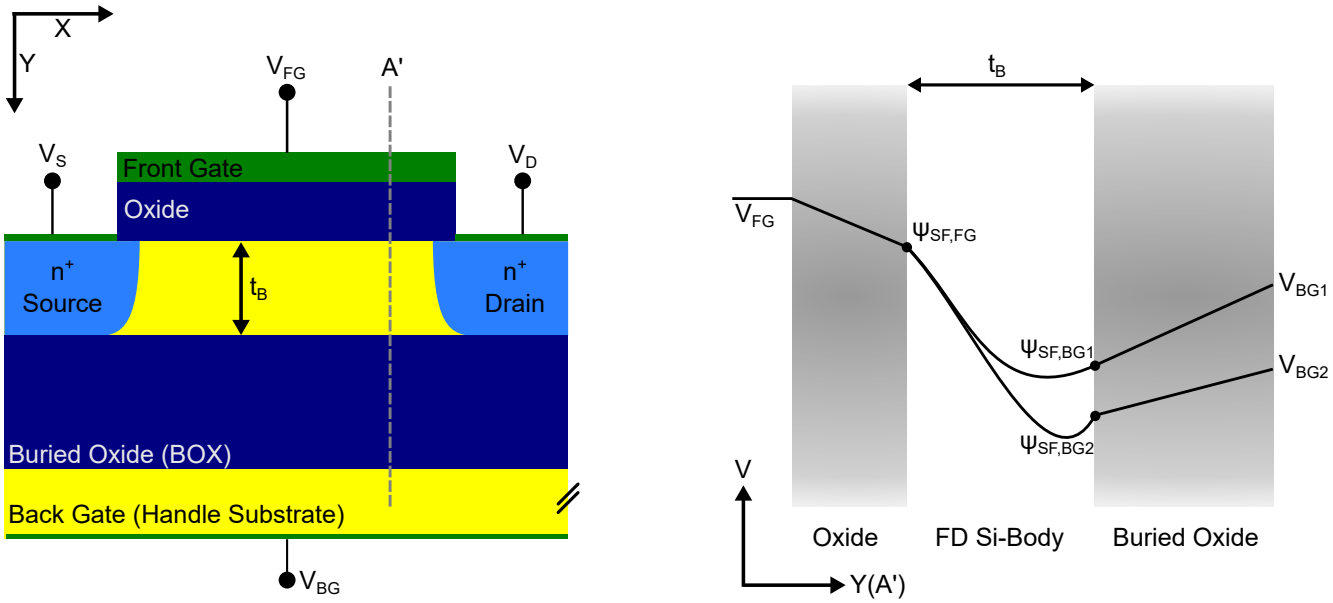
(c) Combined effects of V_{GS} and V_{DS} for MOSFET for transition from off to on-state $V_{GS} > 0\ V$, $V_{DS} > 0\ V$

Fig. 9: Schematic energy band diagrams of the idealized n-type MOSFET under different biasing conditions.

2.3.1 SOI MOSFET

In order to increase the electrostatic control of deeply scaled MOSFET, advanced device structures of increased complexity have been researched and introduced in the semiconductor industry over the last decades. One of these advances is the silicon-on-insulator (SOI) MOSFET as depicted in Fig. 10a [64, 65]. The main benefits of appropriately designed SOI MOSFET include reduced junction leakage, minimized short-channel effects and negligible S/D junction capacitance as well as increased soft-error immunity besides an absence of parasitic latch-up effects in CMOS circuit structures [64]. Compared to the bulk MOSFET (Fig. 8a), an additional buried oxide insulation layer is placed between the handle substrate and the active surface region of the device. Consequently, this structure can feature two gate electrodes, i.e. the front gate and the back gate.

Depending on the thickness (t_B) and dopant concentration ($N_{A/D}$) of the top silicon layer, also known as the *body* layer, partly depleted (PD) and fully depleted (FD) SOI MOSFET are distinguished (Fig. 11) [64, p.156]. As the naming suggests, the FDSOI features a completely depleted body layer whereas PDSOI exhibits a neutral region between the depletion regions at the front

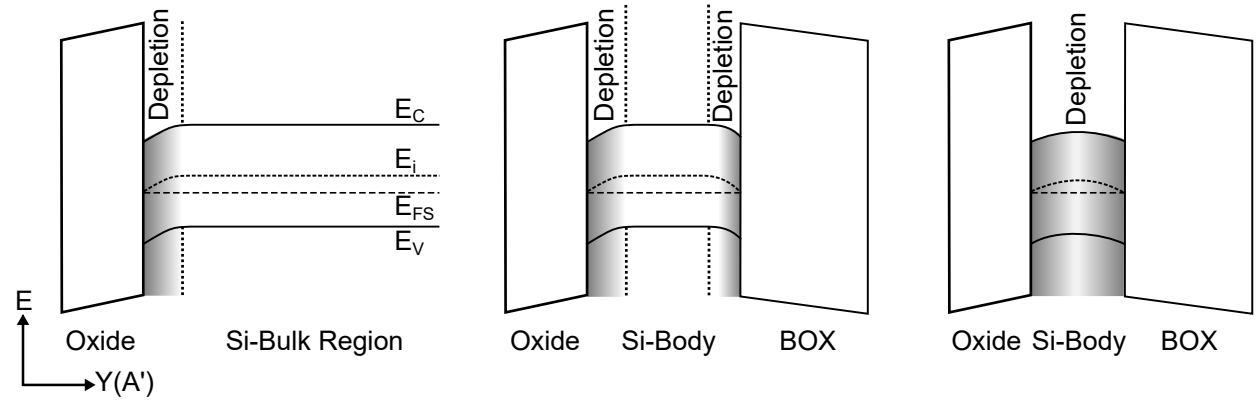


(a) Schematic cross-section of a FD SOI MOSFET structure.

(b) Schematic potential diagram of an idealized SOI MOS capacitor for two back gate biasing conditions modified after Colinge [64, p.160].

Fig. 10: Ideal FD SOI MOSFET structure and corresponding schematic electrostatic potential. V_{FG}, V_{BG} front and back gate potential; $\psi_{\mathrm{SF,FG}}$, $\psi_{\mathrm{SF,BG}}$ surface potential of silicon body induced by front and back gate, respectively; t_{B} body layer thickness.

and back silicon-to-oxide interface at the onset of weak inversion (Fig. 11). Hence, PDSOI MOSFET behave similarly to bulk MOSFET.



(a) Classic MOSCAP on bulk **(b)** Partly depleted SOI **(c)** Fully depleted SOI

Fig. 11: Schematic Energy band diagrams of the bulk and SOI MOSCAP on p-type substrate under weak inversion condition modified after Colinge [64, p.156]. Gate metalization omitted for clarity.

For a sufficiently thin and low-doped top silicon layer an electrostatic coupling of the front and back gate induced surface potentials $\psi_{SF,FG}$ and $\psi_{SF,BG}$ can be observed (Fig. 8b). In this case, the potential curve $\phi(y)$ inside the body layer can be approximated by [64, pp.170],[65, pp.15]:

$$\phi(y) = \frac{qN_{A/D}}{2\kappa_S} y^2 + \left(\frac{\psi_{SF,BG} - \psi_{SF,FG}}{t_B} - \frac{qN_{A/D} t_B}{2\kappa_S} \right) y + \psi_{SF,FG}$$

For this reason, the threshold voltages V_{th} of both gates are electrostatically coupled as well. This enables up to 9 operation modes for FD devices as depicted in Fig. 12. In this thesis, the later discussed electrostatically doped reconfigurable MOSFET FDSOI devices are based on the operation modes of back gate inversion and accumulation combined with front gate modes of inversion, depletion and accumulation. Note, that for a silicon body thickness below ~10 nm and a channel length below ~100 nm, the coexistence of electron and hole charge carriers for simultaneous inversion and accumulation at the respective interfaces is prohibited by the so called supercoupling effect due to an insufficient potential drop over the body layer [66].

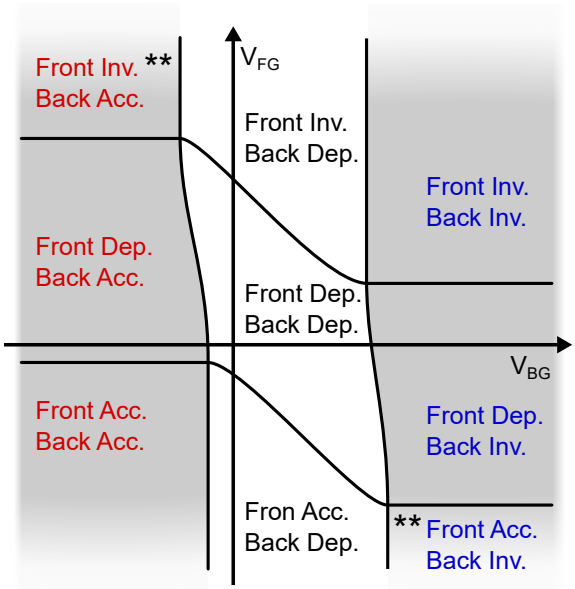


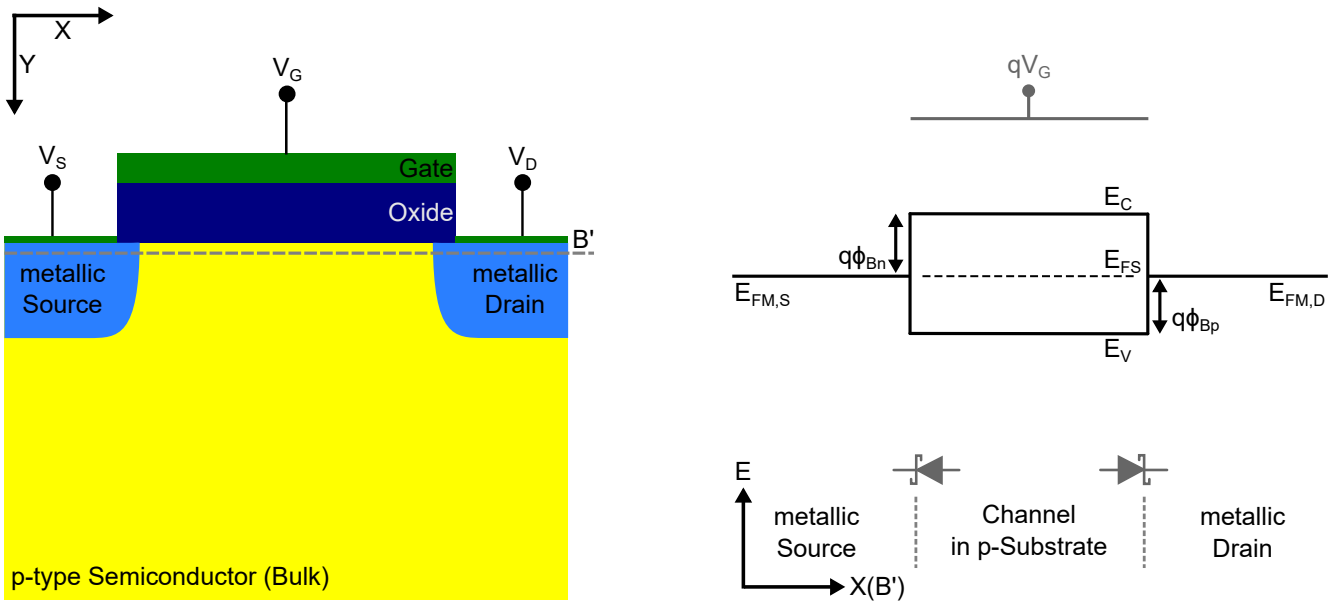
Fig. 12: FD SOI NMOS operation modes as a function of front gate (V_{FG}) and back gate (V_{BG}) biasing for moderately bias V_{DS} after Colinge [64, pp.157]. Grey marked operation modes are used throughout this thesis for electrostatically doped reconfigurable MOSFET devices (red PMOS operation, blue NMOS operation, see following chapter 2.4). **Operation mode affected by supercoupling effect for ultra thin body devices.

2.3.2 Schottky Barrier MOSFET

Schottky barrier FET (SBFET) have been extensively studied in the recent decades motivated by the industrial need for continuous down-scaling of CMOS technology [25, 43, 51, 67]. Es-

pecially in the beginning, the SBFET proved rather difficult to fabricate reproducibly as the Schottky barrier height is quite sensitive to process variations and technological limits of semiconductor processing equipment first had to be overcome [35]. Also, any present potential barrier between the metal and the silicon channel reduces the on-current and results in a poor sub-threshold behavior and therefore increased S/D off-state leakage compared to conventional MOSFET (see sections 2.3.3 and 2.2). Hence, for high-performance SBFET, an effective Schottky barrier height (eSBH) $\ll 0.1\,\mathrm{eV}$ has to be realized as summarized in 2.2.2 (Fig. 7). Nevertheless, the possible advantages of a reduced parasitic gate-overlap capacitance as well as S/D resistance, a low thermal budget and a reduction in channel doping enabling increased channel carrier mobilities as well as atomically abrupt SB junctions for further device scaling continuously fueled the research interest [25, 43, 51, 67].

In comparison to a conventional MOSFET structure (Fig. 8a), the SBFET illustrated in Fig. 13a features metal S/D with atomically abrupt SB junctions instead of conventionally graded p-n junctions.



(a) Schematic Cross-section of an n-type metal-oxide-semiconductor metallic S/D SB field-effect transistor (SBFET) structure.

(b) Schematic energy band diagram of an idealized ambipolar SBFET based on a virtually undoped semiconductor with mid-gap SB metal S/D in thermal equilibrium.

Fig. 13: Schematic SBFET structure and corresponding idealized energy band diagram. V_G gate potential; V_S source potential; V_D drain potential; $E_{FM,S}$, $E_{FM,D}$ metal Fermi energy level at source and drain; E_C bottom edge of the conduction band; E_V top edge of the valence band; q elementary charge.

The basic operating principle of a long-channel SB-MOSFET is illustrated by schematic energy band diagrams in Fig. 14. For the sake of simplicity, the diagrams depict ideal mid-gap SB S/D contacts as it is the case for strong Fermi level pinning or for materials such as NiSi in contact

with an undoped semiconductor [25, 68]. As stated before, high-performance SBFET feature very low specific eSBH (see section 2.2.2) but the general operation principle does apply as well.

Fig. 13b depicts the schematic energy band diagram of the simplistic SBFET in thermal equilibrium. Depending on V_{GS}, the SBFET can behave either as an n- or a p-channel MOSFET. Applying only V_{DS} does not result in a significant current flow between source and drain (I_{DS}) as both charge carriers face the mid-gap potential barrier at the source and drain (S/D) (Fig. 14a,b). For the p-channel operation mode (Fig. 14c,d), V_{GS} has to be sufficiently negative to bend the valence band upwards to reduce the SB widths at either source (c) or drain (d) in order to make the barrier transparent for holes. Note, that the uncommon PMOS biasing of (d) $V_{DS} > 0\ V$ the current I_{DS} and threshold voltage V_{th} depend on the gate-drain voltage instead of the gate-source voltage impeding a channel saturation (see following section 2.3.3).
In case of the n-channel operation (Fig. 14e,f) a positive V_{GS} has to be applied following the same argumentation as for the p-channel. Here, the uncommon NMOS biasing of $V_{DS} < 0\ V$ impedes the channel saturation.

As electrons or holes can form a conducting channel, the mid-gap SBFET is a so called *ambipolar* device enabling transistor level reconfigurability, i.e. selectable or programmable dominant charge carrier type, as discussed in the later following section 2.4.

Non mid-gap SBFET with small eSBH for electrons or holes suppress the carrier injection at the drain to some degree and NMOS as well as PMOS SBFET with comparable performance to conventional MOSFET have been demonstrated by various research groups [25, 42, 43, 51, 56].

2.3.3 Key DC-Parameters of MOSFET

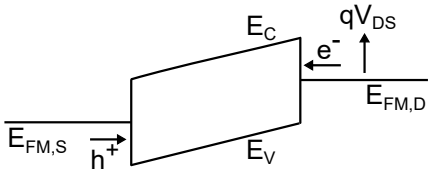
The primary functions of MOSFET devices in integrated circuits are switching and the amplification of voltage signals. In this section, the most important DC characteristics and figures of merit (FOM) of long-channel MOSFET are summarized to facilitate the comparison of different MOSFET designs with regards to their non-ideal switching and amplification behavior.

Drain-Source (Drive) Current I_{DS}

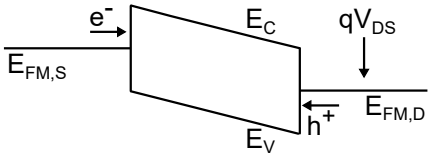
For conventional long-channel[a] MOSFET the drain-source current I_{DS} can be conveniently described by a physically motivated charge-sheet model[b] [19, pp.303],[69]:

[a] Effective channel length $L_G \gg$ space charge region widths W_{SCR} at S/D.

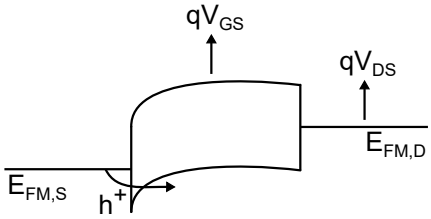
[b] Under the assumption of (1) a one-dimensional potential distribution, i.e. transverse electric field $\mathscr{E}_Y$ (perpendicular to channel) $\gg$ longitudinal electrical field $\mathscr{E}_X$, also known as gradual-channel approximation, and (2) the inversion layer has no extension in Y-direction [69].



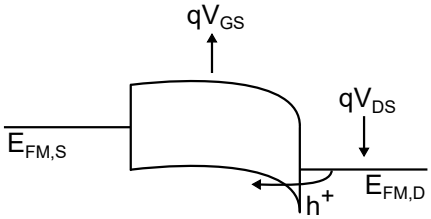
(a) $V_{DS} < 0\ V$, $V_{GS} = 0\ V$, off-state



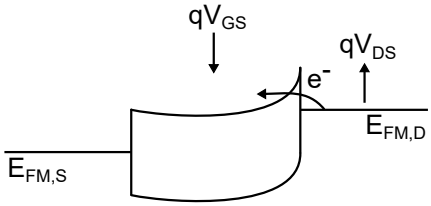
(b) $V_{DS} > 0\ V$, $V_{GS} = 0\ V$, off-state



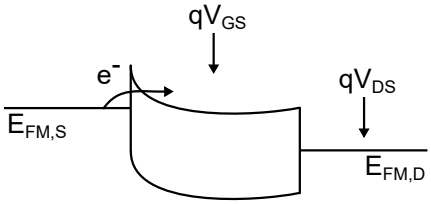
(c) $V_{DS} < 0\ V$, $V_{GS} < 0\ V$,
on-state hole channel



(d) $V_{DS} > 0\ V$, $V_{GS} < 0\ V$,
on-state hole channel



(e) $V_{DS} < 0\ V$, $V_{GS} > 0\ V$,
on-state electron channel



(f) $V_{DS} > 0\ V$, $V_{GS} > 0\ V$,
on-state electron channel

Fig. 14: Schematic energy band diagrams of the idealized ambipolar SBFET under different biasing conditions.

$$I_{DS} = \frac{W_G}{L_G} K \left(\left(V_{GS} - V_{FB} - 2\psi_B - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3} \frac{\sqrt{2\kappa_S \epsilon_0 q N_{A/D}}}{C_{Ox}} \left(\left(V_{DS} + 2\psi_B \right)^{\frac{3}{2}} - \left(2\psi_B \right)^{\frac{3}{2}} \right) \right) \text{ with } K = \mu_{eff} C_{Ox}$$

W_G and L_G are the MOSFET channel width and length, K the technology factor consisting of the effective charge carrier mobility μ_{eff} and the gate oxide capacitance C_{Ox}, V_{FB} the flat-band voltage, ψ_B bulk Fermi level potential, κ_S the permittivity of the semiconductor and $N_{A/D}$ the

acceptor/donator dopant concentration. Note, that μ_{eff} generally is anti proportional to doping concentrations as well as temperature resulting in a reduction of $I_{\text{DS,on}}$ current.

The charge-sheet model illustrates three regions of MOSFET on-state operation for given V_{GS}, i.e. the linear, non-linear and saturation region as depicted in the schematic output characteristic in Fig. 15b.

For very small V_{DS}, i.e. $V_{\text{DS}} \ll (V_{\text{GS}} - V_{\text{th}})$ also known as the linear region, the initial equation reduces to [17, p.184]:

$$I_{\text{DS}} = \frac{W_{\text{G}}}{L_{\text{G}}} K \left(V_{\text{GS}} - V_{\text{th}} \right) V_{\text{DS}} \quad \text{with} \quad V_{\text{th}} = V_{\text{FB}} + 2\psi_{\text{B}} + \frac{\sqrt{2\kappa_{\text{S}} \epsilon_0 q N_{\text{A/D}} (2\psi_{\text{B}})}}{C_{\text{Ox}}}$$

while for small V_{DS}, i.e. $V_{\text{DS}} < (V_{\text{GS}} - V_{\text{th}})$, the equation reduces to:

$$I_{\text{DS}} = \frac{W_{\text{G}}}{L_{\text{G}}} K \left(V_{\text{GS}} - V_{\text{th}} - \frac{V_{\text{DS}}}{2} \right) V_{\text{DS}}$$

Therefore, for small V_{DS} the MOSFET resembles a resistor with a resistivity $R \sim 1/\big(K(V_{\text{GS}} - V_{\text{th}})\big)$, which is controllable by V_{GS}. Notable, the threshold voltage V_{th} depends on the flat-band voltage V_{FB} and is therefore proportional to the gate work function ϕ_{M} (see 2.1). This dependency is exploited in MOSFET device design to realize specifically desired V_{th} values.

A noteworthy distinguishing phenomenon of SBFET is a supra-linear S-shaped output characteristic (green curve in Fig. 15b). This distortion of linearity for very small V_{DS} results from the potential drop across the SB at the drain, which prevents an efficient carrier extraction until the drain forward voltage is sufficiently high. In case of a barrier height smaller than ~$3k_{\text{B}}T$ (~78 mV at 300 K) this effect vanishes and the SBFET behaves like a conventional MOSFET [70].

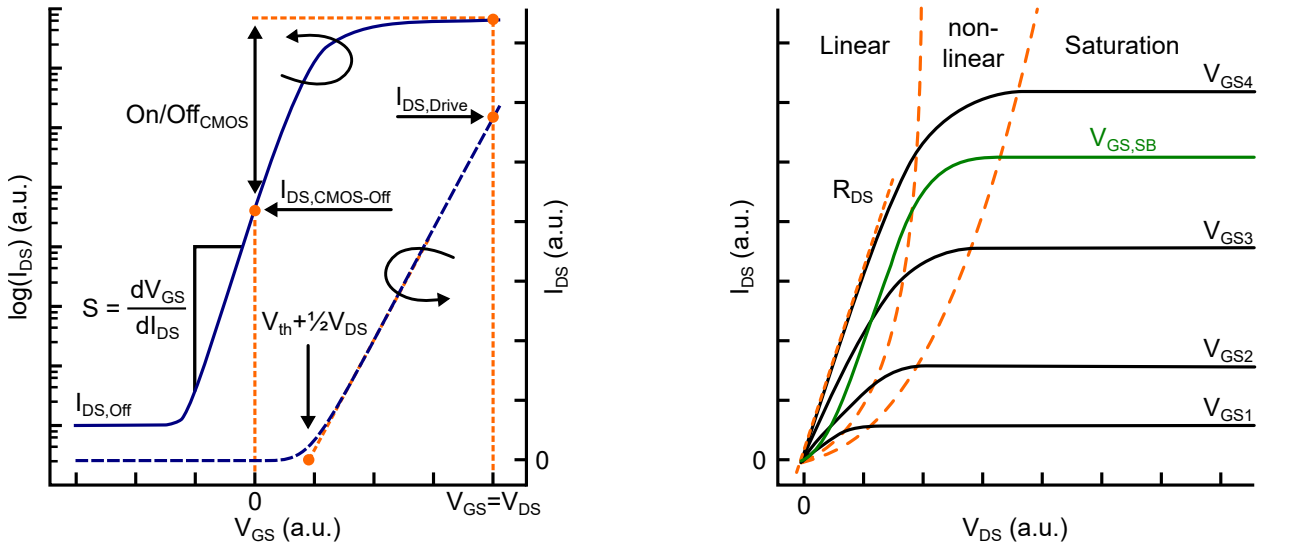
For high V_{DS}, i.e. $V_{\text{DS}} \gg (V_{\text{GS}} - V_{\text{th}})$ also known as the saturation region, the equation reduces to [17, p.186]:

$$I_{\text{DS}} = \frac{W_{\text{G}}}{2L_{\text{G}}} K \big(V_{\text{GS}} - V_{\text{th}} \big)^2$$

In the saturation region, I_{DS} ideally becomes independent of V_{DS} and is solely controlled by V_{GS}.

For conventional integrated CMOS circuits, the highest and lowest possible biasing potentials for MOSFET are fixed by the positive (V_{DD}) and negative (V_{SS} - commonly ground) supply voltage rails. Therefore, relevant CMOS MOSFET parameters are derived for these biasing conditions (Fig. 15a). One of these CMOS parameters is the drive current which is defined as $I_{\text{DS}}(V_{\text{GS}} = V_{\text{DS}})$ and describes the maximum I_{DS} on-current a transistor can provide in CMOS

circuits. Similarly, the minimum achievable off- or leakage current $I_{\mathrm{DS,CMOS-Off}}$ is defined as $I_{\mathrm{DS}}(V_{\mathrm{GS}} = 0)$. A low leakage current and a high on/off$_{\mathrm{CMOS}}$ current ratio are desirable to reduce static power consumption and to increase noise immunity for improved signal integrity of CMOS circuits. The off-current is directly correlated with the sub-threshold swing S and threshold voltage V_{th} which are presented in the following.



(a) Input characteristic $I_{\mathrm{DS}}(V_{\mathrm{GS}})$

(b) Output characteristic $I_{\mathrm{DS}}(V_{\mathrm{DS}})$ of conventional MOSFET (black) and exemplary supra-linear SBFET (green)

Fig. 15: Schematic input and output characteristics of a conventional MOSFET and exemplary output characteristic of a SBFET (green curve).

Threshold Voltage V_{th} and Sub-Threshold Swing S

The threshold voltage V_{th} is possibly one of the most central MOSFET parameters in general. The threshold voltage marks the transition between weak and strong inversion in the channel. For $V_{\mathrm{GS}} > V_{\mathrm{th}}$ the I_{DS} current significantly increases due to the onset of strong inversion in the channel region while for $V_{\mathrm{GS}} < V_{\mathrm{th}}$ the current decreases exponentially marking the sub-threshold voltage (sub-V_{th}) region under weak inversion condition with (Fig. 15a) [17, p.187],[19, pp.314]:

$$I_{\mathrm{DS}} \sim e^{q\left(V_{\mathrm{GS}}-V_{\mathrm{th}}\right)/nk_{\mathrm{B}}T} \quad \text{with} \quad n = \left(1 + C_{\mathrm{Dep}}/C_{\mathrm{Ox}}\right)$$

where C_{Dep} is the depletion layer and C_{Ox} the gate oxide capacitance.

The slope of I_{DS} in the sub-V_{th} region is known as the sub-threshold slope. The inverse of this slope is the sub-threshold swing S which is derived from the input characteristic by

$$S = \left(\frac{d(log(I_{DS}))}{dV_{GS}} \right)^{-1}$$

S is measured in required millivolts of V_{GS} to increase I_{DS} by one decade and quantifies the required V_{GS} span to reach the onset of the on-state or V_{th} from the off-state. Therefore, a steep slope is desirable to reduce the required gate voltage and related gate charge for this transition. For conventional MOSFET the swing is physically limited to approximately 63 mV/dec at room temperature and $65 - 120$ mV/dec are commonly accepted values [71, pp.10]. Hence, V_{th} needs to be adjusted to reduce $I_{DS,CMOS-Off}$ in the sub-V_{th} region while still allowing for a high $I_{DS,Drive}$ in order to realize an optimum in on/off$_{CMOS}$ ratio as well as static and dynamic power dissipation for the given CMOS application, e.g. low power or high performance CMOS circuits.

Depending on V_{th} being positive or negative, two MOSFET operation modes are distinguished. A positive V_{th} describes an *enhancement mode* MOSFET for which the conducting channel is not present at $V_{GS} = 0$ V resulting in transistor off-state. In the case of a negative V_{th}, the conducting channel is already established at $V_{GS} = 0$ V causing transistor on-state. As the channel needs to be depleted in order to reach the off-state this type of MOSFET is named *depletion mode* MOSFET.

As V_{th} is of major importance for MOSFET applications, numerous extraction methods have been developed over time [72, 73]. For instance, the constant current method is widely used in industrial MOSFET fabrication process control to facilitate V_{th} extraction and comparison of V_{th} shifts due to process variations and biasing conditions. Therefore, it is also the preferred approach in this thesis. This method has been extended to reduce the arbitrariness of the reference current level. For instance, it has been proposed to define the reference current to $W_G/L_G x 10^{-7}$ or to define it by the second-derivative method where $d^2 I_{DS}/dV_{GS}{}^2$ exhibits a maximum [73]. Another common traditional method is the linear extrapolation in the linear region, often referred to as extrapolated V_{th}. Here, V_{th} is derived by finding the V_{GS} axis interception point $V_{GS}(I_{DS} = 0$ A), of the linear extrapolation of the input characteristic at its highest slope, i.e. the point of maximum transconductance, and adding $V_{DS}/2$ (Fig. 15a). But, this method is sensitive to parasitic series resistances and mobility degradation effects. To overcome this sensitivity, the popular second-derivative method, also known as transconductance change method, has been developed. This method determines V_{th} as the V_{GS} value where the derivative of the transconductance or the second derivative of the input characteristic exhibits a maximum. Because of

the second derivative taking on the MOSFET input characteristic, this method is quite sensitive to measurement noise and might require numerical smoothing algorithms.

2.4 Electrostatically Doped Reconfigurable MOSFET Concepts

In the last decade several research groups began to develop *electrostatically doped* polarity controllable FET concepts better known as reconfigurable field effect transistors (RFET), that are capable of switching between n- to p-type behavior. This transistor level reconfigurability is able to circumvent some of the fundamental limitations of conventional CMOS technologies while making a reduction of costs per basic implemented logic function feasible [3, 14, 74]. Besides silicon based technologies, reconfigurability has also been demonstrated for new semiconductor materials such as carbon nanotubes [75, 76], mono-layer transition metal dichalcogenides, e.g. WSe_2 and $MoTe_2$ [77–80], and graphene [7]. All these demonstrated concepts share the basic principle of implementing local potential barriers for both types of charge carriers, i.e. electrons and holes, in a low or non-doped semiconductor via external electrical fields, also known as electrostatic doping (ED) [14].

In general, ED refers to the approach of implementing an electrostatic interaction between a semiconductor and a biased or unbiased material with a different work function in order to induce and control the carrier density at the interface [3]. Lately, the research interest in general ED increased as conventional impurity doping for the incorporation of high doping gradients at the single digit nanometer scale is challenging [8, 81]. Especially random dopant fluctuations leading to device variability are considered as a key concern for high yielding manufacturability of nanoscale devices, e.g. nanowires and FinFET, in ULSI circuits [82–87]. Also, the requirements of nanoscale devices for high carrier densities paired with high carrier mobilities point towards impurity free doping solutions. On the contrary, ED offers extremely sharp junctions with a well controllable and adjustable carrier concentration profile as well as a reduced defect density. But, more extensive experimental investigation is needed to confirm and evaluate the competitiveness to mainstream Si-CMOS although calibrated simulations suggest performance benefits especially for SBFET devices [3, 4]. A recent overview on ED structures and concepts is given by Gupta et al. in [3] and a comparison of ED and other alternatives to conventional doping is given by Riederer et al. in [8].

In this work, the focus is laid on silicon based RFET utilizing bias-induced ED via multi-gate structures based on mid-gap Schottky barrier (SB) contacts instead of conventional impurity doped p-n junctions at the source and drain interfaces. The reported Si-RFET device structures mainly differ in the fabrication approach, i.e. bottom-up or top-down process technology, and in the number, positioning and combination of gate electrodes. In all approaches, the gates are electrostatically coupled to a non- or lowly doped silicon channel and to the SB interfaces

of source and drain. This results in the individual control over the injected charge carrier type for unipolar behavior, and over the carrier conduction [14, 74]. The gate for controlling the dominant carrier or the absence of the undesired carrier type is referred to as *program* or *polarity gate* (PG) where as the gate for controlling the carrier conduction is commonly named *control gate* (CG). Note, that the majority of publications in this field is focused on extending end-of-roadmap *silicon nanowire* and *gate-all-around* FET structures while the work presented here considers the less ambitious possibility of leveraging the economically successful and matured planar FDSOI technology [1, 15, 88].

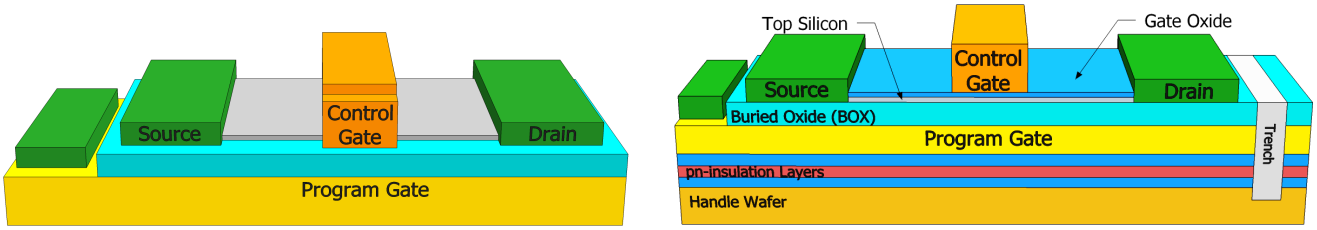
At least two electrically independently controllable gate electrodes are required for transistor level reconfigurability and two general distinguishable approaches for the realization of an RFET based on their carrier flow control mechanism have been demonstrated. For a conceptual comparison of the approaches their schematic band diagrams are depicted in Fig. 17d-k. The actual injection mechanisms of charge carriers through and over the mid-gap SB is described in more detail in section 2.2.1.

The first nanowire (NW) RFET realization has been reported by Koo et al. (2005) followed by Colli et al. (2009) and Wessely et al. (2010) (Fig. 17a) [9–11]. Using a SOI technology, the PG or back gate (BG) is located below the whole channel region while the CG or front gate (FG) is positioned on the top side in the center of the device (Fig. 17a). In this configuration the PG defines the dominant charge carrier type in the device by simultaneously influencing the SB at source and drain while the centered CG determines the current flow (Fig. 17d,f,h,j). By applying a negative (positive) potential to the PG, holes (electrons) are accumulated inside the device. Biasing the CG with an opposite potential induces a potential barrier in the channel and modulates the current flow (Fig. 17f,j). Effectively, charge carriers with lower energies than the potential barrier height are blocked by the CG similar to conventional MOSFET operation.
A related approach using three gate electrodes on stacked silicon NW has been demonstrated by De Marchi et al. and by Mongillo et al. (Fig. 17b) [89–92]. The electrostatic operation principle is similar to the previously described single NW approach (Fig. 17d,f,h,j).

A second approach for the realization of a NW RFET was demonstrated by Heinzig et al. and Weber et al. based on two electrically separated gate electrodes positioned over the source and drain SB contact regions in a bottom-up fabrication process (Fig. 17c) [93, 94]. In this configuration, the PG selectively suppresses the injection of the undesired charge carrier type while the CG determines the amount of current flowing through the device based on the opposite carrier type. For a negative PG and V_{DS} biasing, electrons are blocked at the drain SB contact while for a negative (positive) CG biasing holes are injected (blocked) at the source SB contact resulting in PMOS behavior (Fig. 17e,g). For opposite biasing conditions, NMOS behavior is obtained as illustrated by the band diagrams in Fig. 17i,k. Noteworthy, in this concept the charge carriers

are blocked at the junctions in off-state before actually entering and accumulating the active device region resulting in low S/D leakage currents for moderate operating temperatures.

Based on the pioneering research at the ISTN on NW RFET devices by Wessely et al., that resulted in the first experimental demonstration of an RFET CMOS inverter, a *planar* RFET technology named *dehancement mode*[a] FET technology (DeFET) has been developed and filed for patent (Fig. 16) [11, 12, 16, 95–99].



(a) Schematic cross-section of a planar DeFET **(b)** Proposed pnp-insulated program gate

Fig. 16: Schematic DeFET structures.

As for the NW RFET devices, a SOI substrate is used and the program or back gate is placed below the whole channel as well as the S/D SB contacts affecting the source and drain SB simultaneously in order to select the dominant charge carrier type in the top silicon body layer. Furthermore, the electrical field of the program gate attracts the dominant charge carriers to the buried oxide interface forming a continuous electron or hole charge carrier channel between source and drain. Again, the control or front gate determines the amount of current flowing through the device by locally depleting the channel and the electrostatic operation principle is similar to the single NW concept (Fig. 17a,d,f,h,j).

The key features of the DeFET structure in comparison to the other RFET concepts, besides its reconfigurability, are the reduced fabrication complexity and the on-the-fly threshold voltage shift-ability over a wide range via the insulated program electrode granting circuit designers additional flexibility [15, 88, 98]. Also, very high operating temperature robustness paired with low $I_{DS,off}$ current leakage has been experimentally demonstrated [95, 100]. Furthermore, the parasitic S/D to gate capacitance of the control gate is minimized because of the non existing S/D-overlap benefiting high operating frequencies. The basic concept of the planar RFET has lately been verified by Yojo et al. although the authors have missed key design considerations for further device optimization [101, 102]. Further, using multi-BOX SOI or less technologically complex pnp-insulated wells for individual back gate insulation via trench isolation large scale integration based on current FDSOI nodes seems feasible (Fig. 16b). Finally, it has been proposed and lately experimentally realized to integrate memory functions into RFET devices for the implementation of 'learning' devices and networks [101, 103, 104].

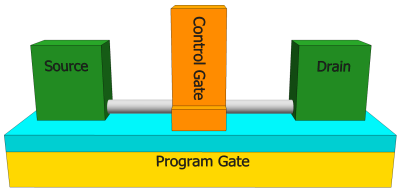
[a] The naming is derived from the intrinsic combination of depletion and enhancement mode operation in one device as discussed in 3.2.

More sophisticated DeFET structures feature additional gate or field-plate electrodes on the top side of the S/D SB in order to proposedly increase the on-current capability while reducing the static CMOS off-state leakage current by increasing the threshold voltage due to a reduction of required back gate potential [97, 105].

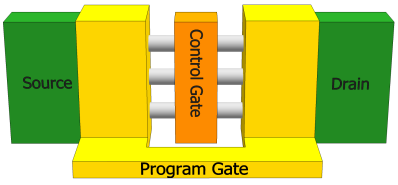
In general, the RFET concepts are capable of enhancing electronics by increasing performance and functional value although being suspected to generally deliver lower drive currents and therefore increased intrinsic switching delays compared to conventional state-of-the-art MOSFET [106]. However, RFET offer a higher expressive capability at the logic circuit level reducing the number of needed transistors for a given logic function and altering the circuit topology in terms of delay and power consumption [13, 14, 89, 92, 107]. The basic logic NOT-function or inverter based on RFET devices has first been experimentally demonstrated by Wessely et al. [12, 98] and later by De Marchi et al. [89]. Up to date, three different approaches to realize the higher expressive capability of RFET on the logic gate level have been explored. The approaches are based on the RFET intrinsic exclusive-or functionality, the equivalence of pull-up and pull-down networks in conjunction with DeMorgan's law and the possibility to merge serial branches into a single RFET device with individual control gates. An overview of RFET based CMOS circuit design and its application, besides others, in hardware security and resilience as well as self-checking logic circuits is given by Mikolajick et al. in [14] and by Gaillardon et al. in [13].

In order to implement RFET into today's energy efficient circuit design based on complementary n- and p-type transistors, i.e. CMOS circuit technology, special device design considerations have to be fulfilled. In the static case in ideal CMOS circuits only one connection to the supply voltage rails is conducting, i.e. either the pull-up (p-type) or pull-down (n-type) network, while the other connection is in a high impedance state. Hence, the total power consumption resulting from current flows only originates from dynamic switching events. In order to obtain high performance CMOS circuits, p- and n-type transistors need to be as symmetric as possible in terms of drive current, threshold voltage and switching slope. Albeit, in the majority of real semiconductors the inherent asymmetry of the conduction and valence energy bands results in differences in carrier conduction and injection behavior for electrons and holes. Therefore, specific optimizations for n- and p-type transistors are common practice in the conventional CMOS technology including channel width adjustment for drive current symmetry, gate work function tuning and even the implementation of different dielectric materials for compensating slope and threshold voltage asymmetries [14, 107, 108]. All these optimization strategies are not available in RFET based CMOS circuits as the very same physical device is required to establish p- or n-type behavior on demand and therefore RFET need to provide intrinsically symmetrical properties for both carrier types.

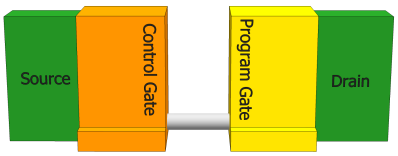
As RFET are based on mid-gap SB contacts, the on-state or drive current is mainly depending on tunneling probabilities through the SB (see 2.2.1). Tuning of the tunneling probabilities is possible by applying mechanical stress [109] or by adjusting the S/D work function in conjunction with silicidation induced dopant segregation (SIDS) in order to manipulate the energy band structure (see 2.2.2). The later method is discussed in more detail in the following experimental section 3.2.



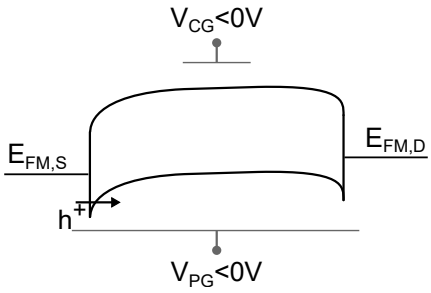
(a) Global PG via a common back gate electrode and CG centered in the channel region [11]



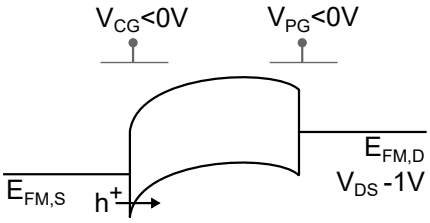
(b) Stacked NW FET with PG over the S/D SB contacts and CG centered in the channel region [89–91]



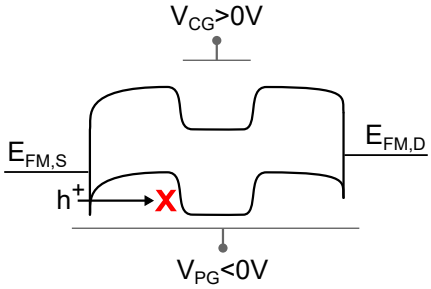
(c) PG and CG separately placed over S/D SB contacts [93, 94]



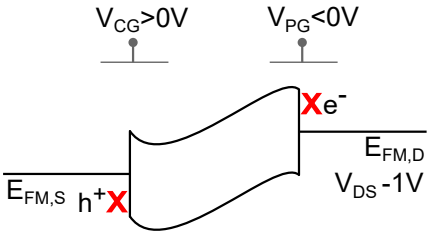
(d) PMOS on-state for a) and b)



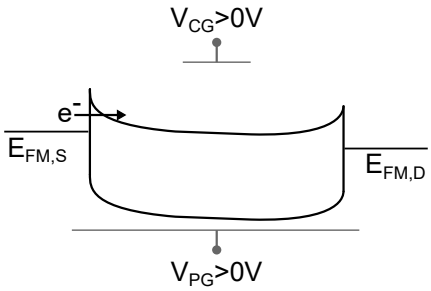
(e) PMOS on-state for c)



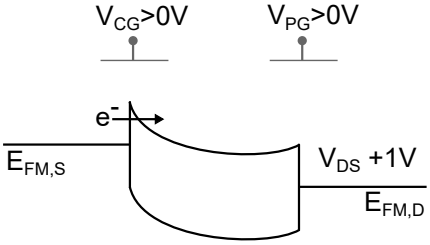
(f) PMOS off-state for a) and b)



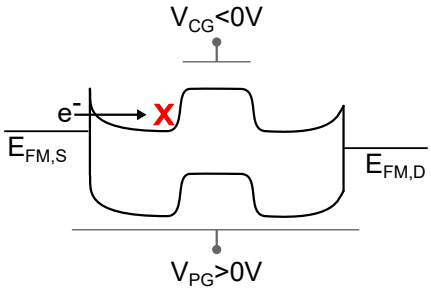
(g) PMOS off-state for c)



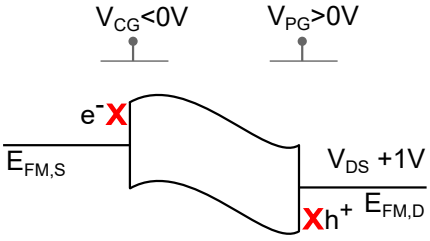
(h) NMOS on-state for a) and b)



(i) NMOS on-state for c)



(j) NMOS off-state for a) and b)



(k) NMOS off-state for c)

Fig. 17: NW RFET approaches with corresponding schematic band diagrams (q omitted for clarity).

3 Experimental Proof-of-Concept and TCAD Simulation

3.1 Device Fabrication Process

The developed proof-of-concept (POC) fabrication process is designed for robustness, flexibility and comparably reduced requirements on semiconductor processing facilities. In order to obtain a high design flexibility a non-self-aligned gate process is selected to fabricate the long-channel RFET devices in the range of 2 to 100 µm gate length. The fabricated devices are based on Soitec Smart Cut^{TM} 8 inch SOI substrates with an initial 70 nm top silicon body thickness over a 145 nm burried oxide insulation layer (BOX)[110].

The fabrication process commences with a RCA standard cleaning of the 2 inch SOI wafers in order to remove possible organic and metallic contamination. Thereafter, a hardmask stack is applied on the beforehand HF stripped Si-body surface consisting of a dry oxidized stress relief SiO_2 layer (6.5 nm), a chemical vapor deposited (CVD) silicon nitride layer (30 nm) and a final SiO_2 layer (3 nm) formed by wet oxidation of the silicon nitride layer at 950°C [111] (Fig. 18a).[a]

Successive optical lithography and wet etching process steps are applied in order to form a H-shaped mesa structure on top of the BOX layer electrically isolating the individual transistors (Fig. 18b). The lithography is based on the common AZ5214 multi-purpose resist enabling negative lift-off as well as positive and negative direct pattern transfer [112]. The central channel region is recessed by TMAH etching and finally trimmed in thickness by dry thermal oxidation (Fig. 18c, d). A dry thermal oxidation step at 1145°C for 40 seconds is applied to form the FG_{Ox} SiO_2 layer of 7.8 nm (Fig. 18e).

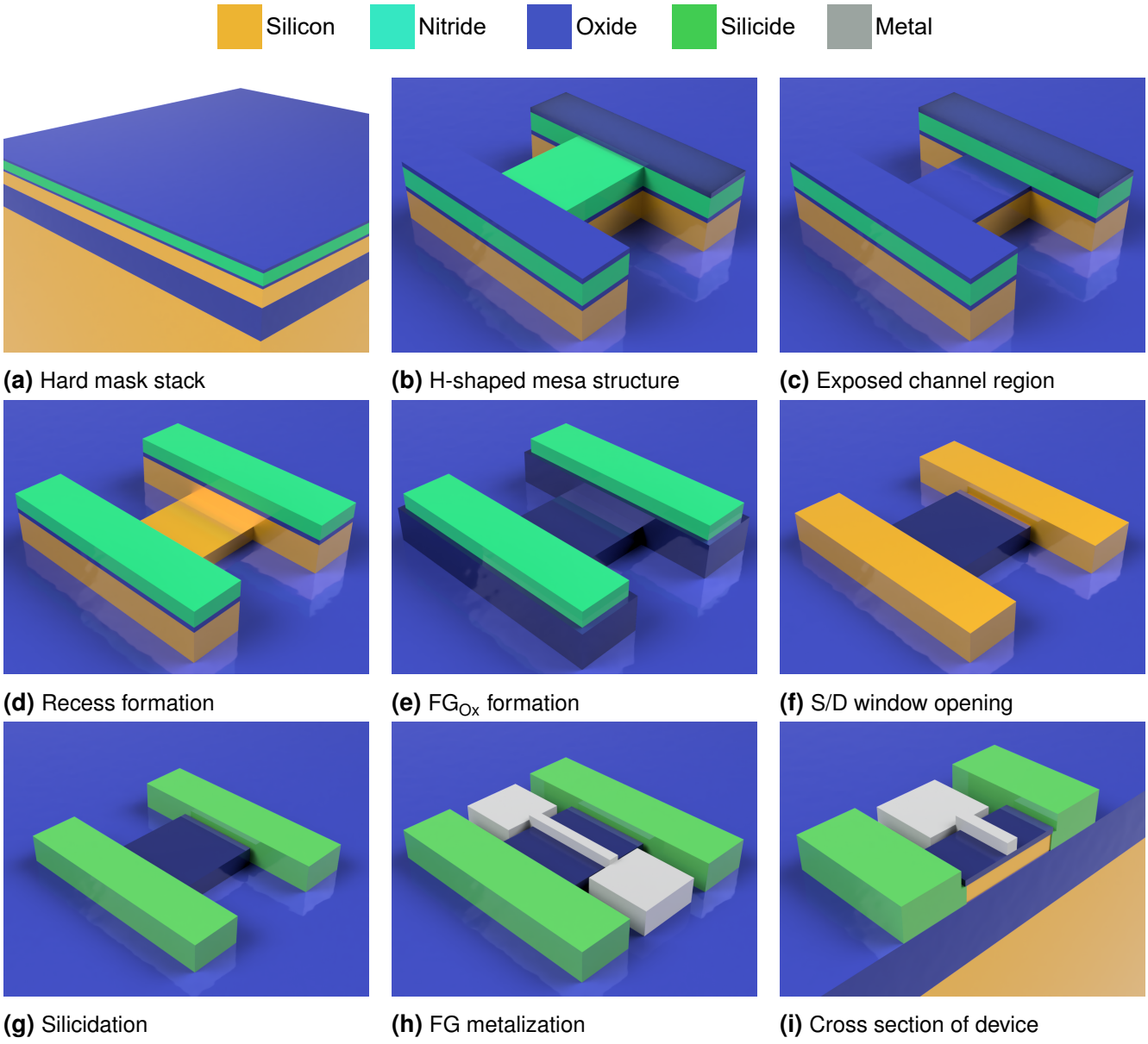
The metalization layers are fabricated by means of lift-off lithography in conjunction with electron beam and sputtering as physical vapor deposition (PVD) processes. For the S/D SB formation a layer of 100 nm nickel is applied by electron beam PVD and annealed in later described processes in order to form nickel silicide phases, i.e. Ni_2Si and NiSi, with varying dopant pile up profiles (Fig. 18f, g).

The FG electrode consists of either electron beam evaporated aluminum or nickel as well as reactively DC magnetron sputter deposited tungsten-titanium-nitride ($WTiN_x$) (Fig. 18h, i).

The reactive sputtering deposition is based on a tungsten-titanium 90/10 wt% target and a sputtering gas mixture of 33:3 mm Ar:N_2 as empirical set-points on gas rotameters [113, 114]. In order to reduce the high energy particle bombardment of the gate oxide, a plasma charge trap is preemptively introduced [115]. The successful nitridation results in a semi-transparent layer of 100 nm thickness as illustrated in Fig. 19c, d.[b] Devices with dual-metal FG electrode are designed by covering the first by a second metalization layer, i.e. capping. The resulting FG metalizations are depicted in Fig. 19 and Fig. 20.

[a] Layer thickness process controlled by ellipsometer and/or profilometer.

[b] For comparison, WTi films of 100 nm are opaque (not shown here).

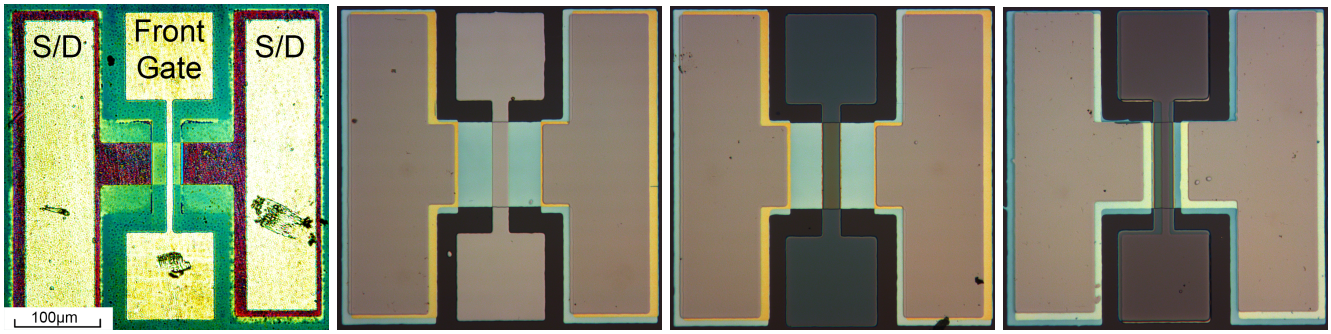


(a) Hard mask stack **(b)** H-shaped mesa structure **(c)** Exposed channel region

(d) Recess formation **(e)** FG_{Ox} formation **(f)** S/D window opening

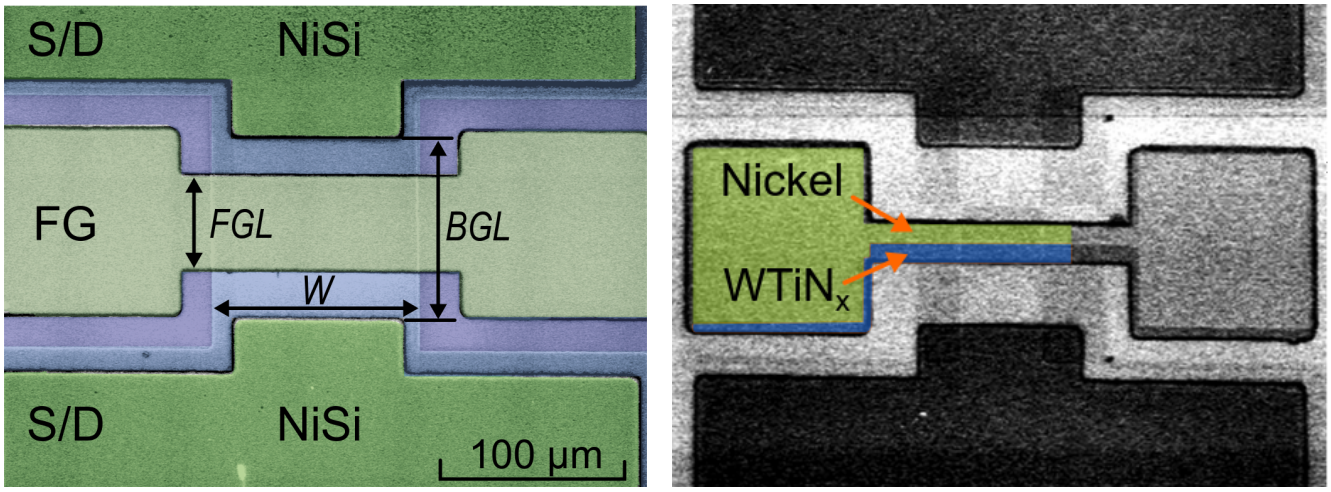
(g) Silicidation **(h)** FG metalization **(i)** Cross section of device

Fig. 18: Main fabrication process steps.



(a) 1st gen. Al FG. **(b)** 2nd gen. Ni FG. **(c)** 2nd gen. $WTiN_x$ FG. **(d)** 2nd gen. Ni/$WTiN_x$ FG.

Fig. 19: Top view micro-graphs of Aluminum, Nickel, Tungsten-Titanium-Nitride and Nickel/Tungsten-Titanium-Nitride dual-metal FG devices from left to right .



(a) Nickel FG device. 700x magnification
Back, front gate length (BGL, FGL) and width (W)

(b) Dual-metal FG (Ni/WTiN$_x$) device
300x magnification

Fig. 20: Top view SEM pictures of fabricated devices (300x magnification, false colored).

Two different silicidation processes are introduced to form different SB characteristics at the S/D contacts. A single silicidation process step in a horizontal furnace at 420°C for 2x 300 seconds in forming gas atmosphere (10:90 H_2:N_2) is applied to the 1st device generation. During the silicidation, the NiSi phase extends into the channel region and forms a NiSi interface with a considerable boron pile up at the Si/NiSi interface as described in subchapter 2.2.2. This process was firstly introduced by Dr. F. Wessely at the ISTN and was part of the predecessor nanowire RFET technology [16].

Alternatively, a two temperature silicidation process is applied to the 2nd device generation. Firstly, a Ni_2Si phase is formed in a soak silicidation process at 280°C for 320 seconds in total. This temperature step is known to form a Ni_2Si layer as long as the nickel layer is not completely consumed [63, 116]. The excessive nickel is selectively stripped by a diluted piranha[a] etch. Secondly, a RTA silicidation step at 410°C for 120 seconds in total is applied to one split of sample wafer TK3-13 triggering a phase transition of Ni_2Si to NiSi [61, 63, 117]. In between the silicidation process steps, monitor devices are electrically characterized to confirm the SB formation as discussed in the following section 3.2. At the end of the day, transistors with Ni_2Si and NiSi SB S/D interfaces with significant and fine tuned boron pile up are obtained from the RTA and furnace based silicidation process schemes.

The 4x4 test dice per wafer mask layout is depicted in Fig. 21. Several transistor widths from 5 to 100 µm with BGL from 30 to 100 µm and FGL between 2 and 80 µm are included (Fig. 20b). Also, different FG positions inside the BGL region as well as BG-only (or pseudo FET [118]) devices with and without recess are part of the device matrix. A sketch of the wafer level design of experiments and a top view of the processed wafer TK3-13 are depicted in Fig. 22.

[a] Recipe: 4 parts H_2SO_4, 1 part H_2O_2, 60 parts H_20

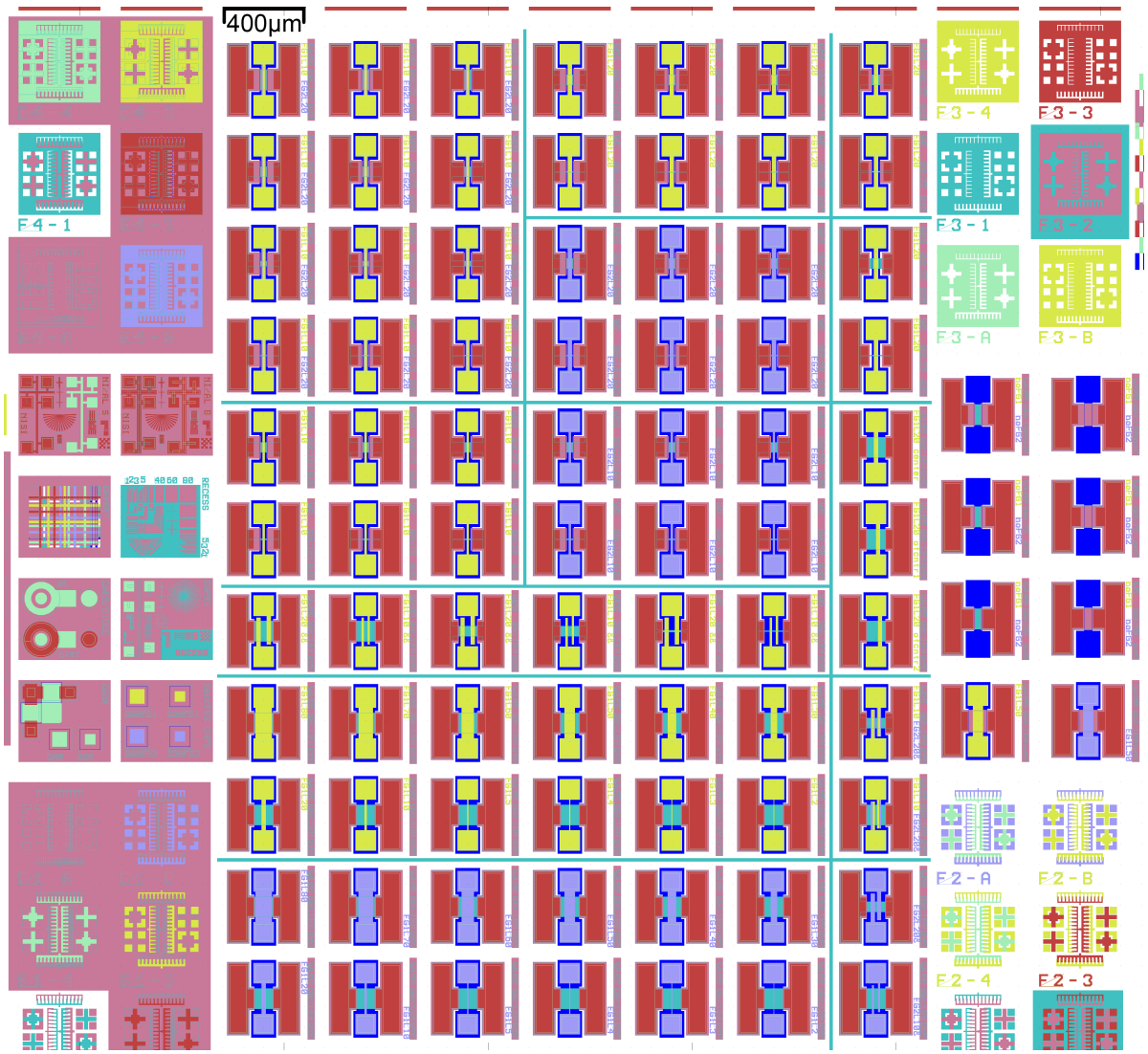
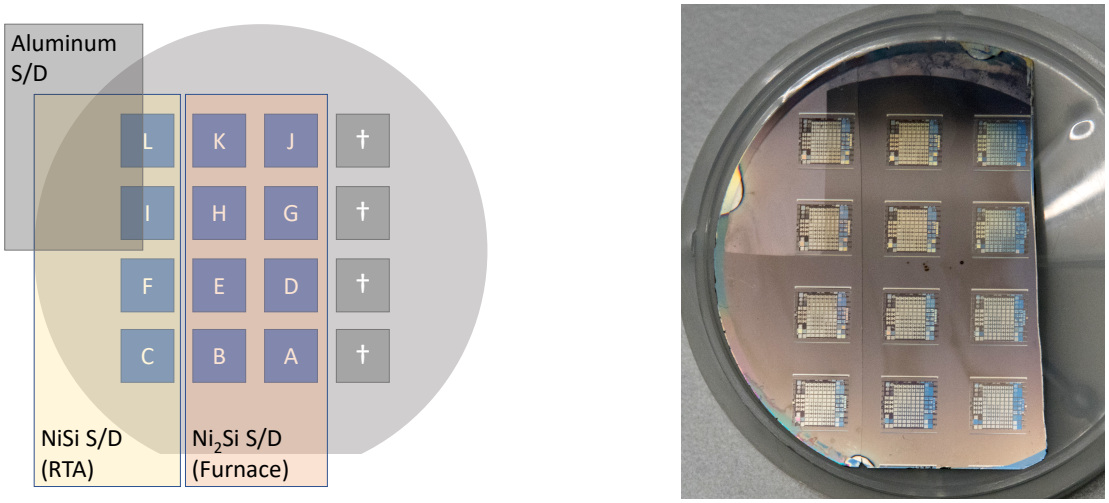


Fig. 21: Mask layout of test dice.



(a) Split wafer segments

(b) Processed 2“ wafer top view

Fig. 22: Wafer level design of experiments.

3.2 Device Characterization and Simulation

In the first part of this chapter, the operation principles and relevant device operation biasing conditions are presented based on electrical characterizations of dual-independent-gate long-channel proof of concept (POC) RFET devices. Thereafter, a TCAD device simulation is introduced in order to further illustrate the device concept. The simulation results are derived by the commercial *Synopsys Sentaurus Device* (v2017-09 SP1) [119] simulator based on the framework presented by Schwarz et al. [21, 22]. In the second part, the effects of various design parameters are discussed and compared based on a simulated scaled self-aligned reference device featuring symmetric p- and n-type properties. Experimental long-channel device characterization results are referenced and compared where applicable as no scaled self-aligned POC devices are available at this point. In addition, the POC device high operating temperature characteristics are presented in the third part. In the fourth and last section, as part of an outlook, an advanced RFET device structure is proposed and compared to the reference device in order to demonstrate the optimization potential of the presented RFET device concept.

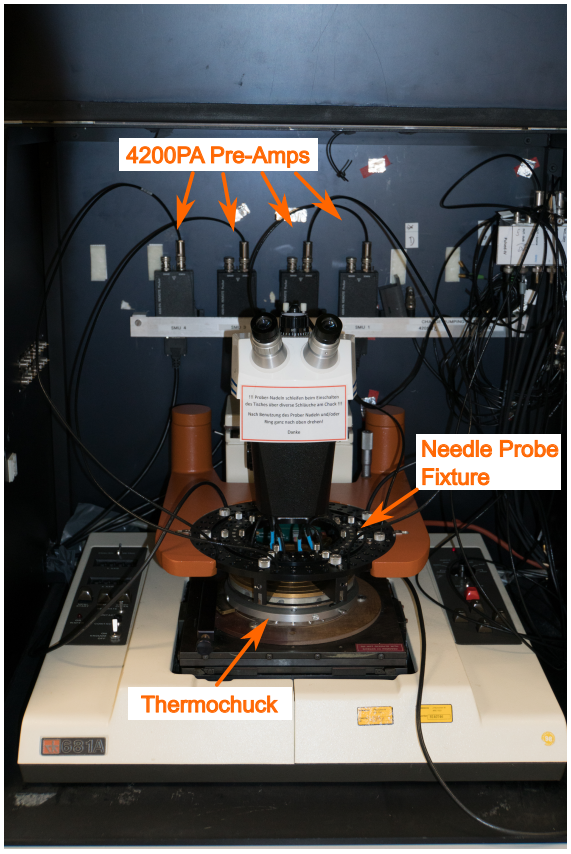
All electrical characterization results have been obtained via a 4200-SCS Keithley Instruments semiconductor parameter analyzer equipped with 4200-PA remote pre-amplifiers in a dark-box enclosure (Fig. 23a,b). All measurements have been conducted on wafer level using a semi-automatic Rockers & Kolls wafer prober, which is equipped with a Thermotronic high temperature wafer chuck and adjustable tungsten probe tips (Fig. 23c,d). In order to characterize the individual devices under test (DUT), the wafer is placed on the wafer chuck and locked by applying a backside vacuum. Subsequently, the electrical contacts are realized by the tungsten probe tips from the top side to the source and drain (S/D) as well as the front gate (FG) and by the chuck at the backside of the wafer to the back gate (BG).

3.2.1 Long-Channel Dual-Independent-Gate DeFET

The here discussed RFET device can be considered as an intrinsic composition of two entangled transistors, i.e. a depletion mode FET on top of an enhancement mode SBFET (Fig. 24). Therefore, the naming *dehancement mode*[a] MOSFET (DeFET) for this RFET concept is introduced here.

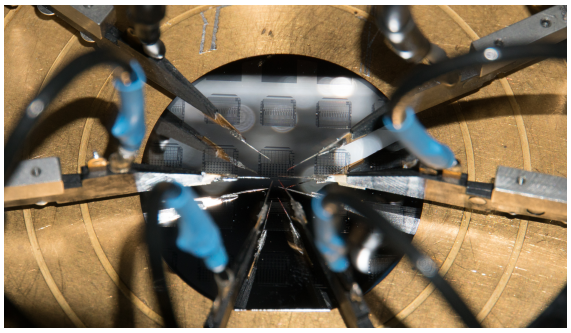
Each of these two transistors is represented by its own gate electrode, namely the front gate (FG) and the back gate (BG). Another common naming convention in the context of RFET devices is program or polarity gate (here the BG) and control gate (here the FG) (see subchapter 2.4).

[a] after Dr.-Ing. Ralf Endres

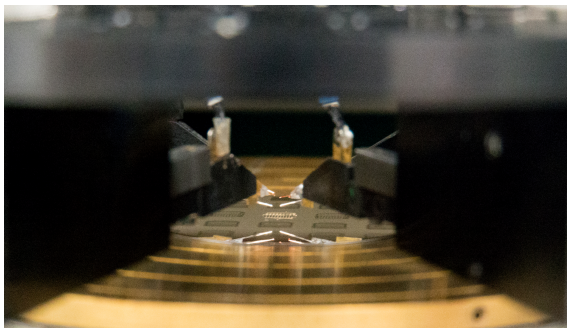


(a) Wafer prober setup in dark-box enclosure

(b) Keithley 4200-SCS parameter analyzer rack



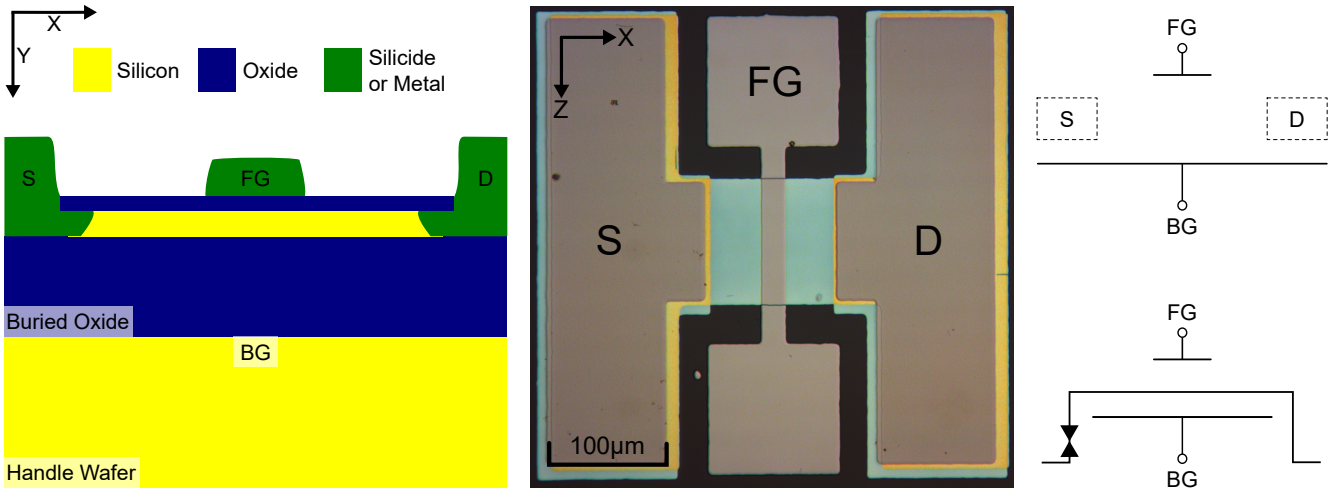
(c) Tungsten probe needle fixture top view



(d) Tungsten probe needle fixture side view

Fig. 23: Electrical characterization setup based on a Keithley Instruments 4200-SCS semiconductor parameter analyzer and Rucker & Kolls waferprober equipped with a high temperature wafer chuck.

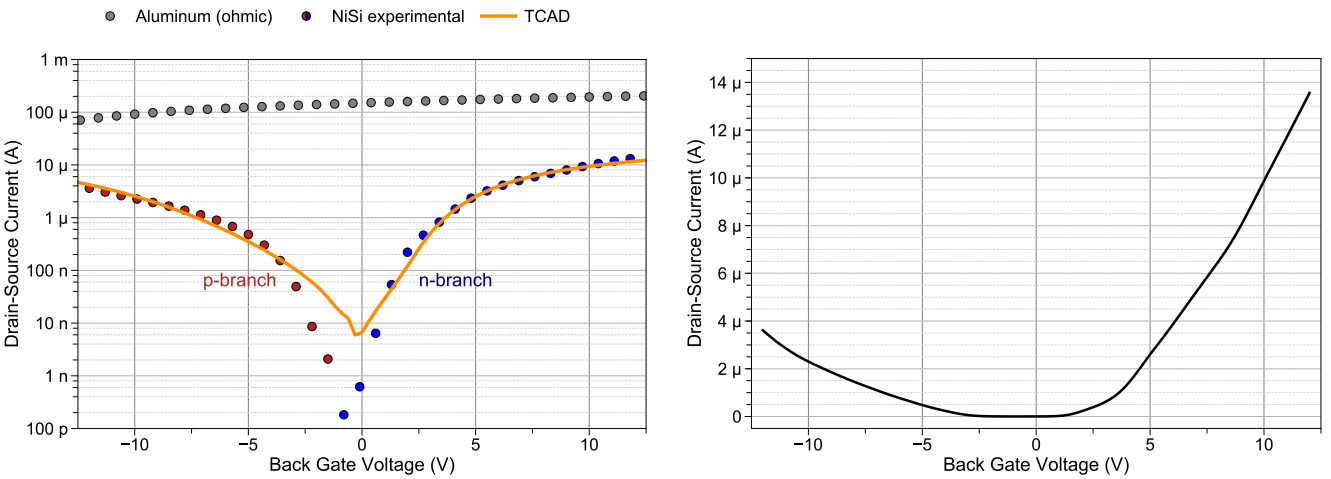
The BG electrode forms an ambipolar buried channel pseudo SBFET [118] and electrostatically influences the whole channel region, i.e. the Si-body layer and especially the SB contacts at source and drain (S/D). Fig. 25 depicts the BG-only (FG electrode omitted) input characteristics exhibiting a clear ambipolar enhancement mode or normally-off behavior. Applying a sufficiently high BG voltage (V_{BG}) results in an increasing drain-source current (I_{DS}) as either holes ($V_{\mathrm{BG}} \ll 0\,\mathrm{V}$) or electrons ($V_{\mathrm{BG}} \gg 0\,\mathrm{V}$) are injected and attracted to the body-silicon-to-BOX interface forming the conductive channel.



(a) Schematic cross section **(b)** Top view micrograph **(c)** Symbolic

Fig. 24: Illustrations of the experimental dual-gate POC device (see also Fig. 20 and Fig. 19).

In order to further illustrate the device operation, TCAD simulations have been conducted based on the schematic long-channel structure depicted in Fig. 26. The device dimensions and composition are related to the experimental device depicted in Fig. 24 and Fig. 20 (see 3.1). However, the long-channel simulation setup has to be regarded as scaled by an order of magnitude in comparison to POC devices in order to keep computational effort at bay.



(a) Logarithmic plot **(b)** Linear plot, NiSi experimental

Fig. 25: Measured and simulated BG input characteristics of a pseudo BG-only SBFET with mid-gap NiSi SB contacts at 323 K and $V_{DS} = -1$ V.
Experimental Device Dimensions: BGL 50 µm, Width 100 µm.

The simulated device consists of an SOI substrate with a BOX thickness of 145 nm, a Si-body thickness (t_B) of 10 nm and a FG_{Ox} thickness of 7 nm SiO_2. The lateral dimension of the FG (FGL) is 1 µm with a FG underlap (negative overlap) of 0.6 µm to the source and drain SB contacts. Consequently, the BG has a length (BGL) of 2.2 µm. The work function of the FG

electrode is specified to mid-gap 4.66 eV. The Si-body layer and handle wafer are p-type doped with a boron concentration of 1e15 cm^{-3}. The Schottky barrier height for holes at source and drain is calibrated to an almost mid-gap level of $\phi_{Bp} = 0.4\,eV$ ($\phi_{Bn} = 0.71\,eV$) enabling device-level reconfigurability as described in subchapter 2.4. A boron pile-up based on silicidation induced dopant segregation with a peak concentration of 8e17 cm^{-3} following an error function profile is assumed to be present in the body layer at the SB interfaces.

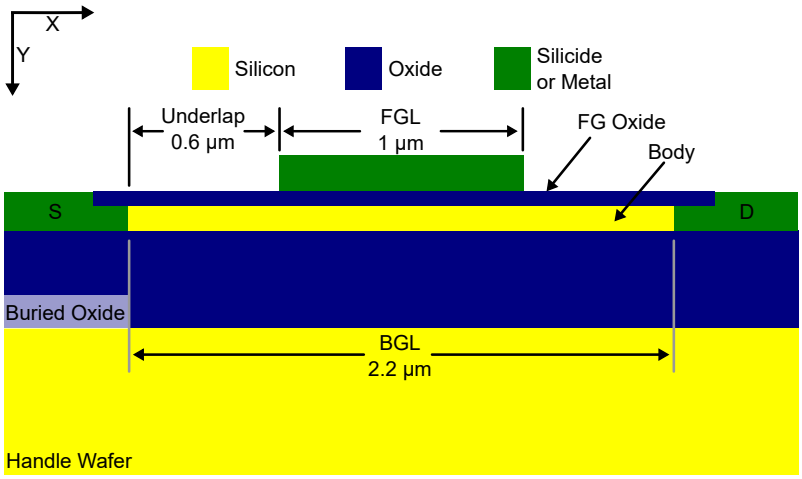


Fig. 26: Schematic structure of the simulated long-channel dual-gate DeFET device (not to scale).

A detailed calibration of the device simulation against POC long-channel devices is technically challenging as hardly avoidable process variations on an academic level result in moving targets for geometrical and chemical parameters. For instance, the silicide interface shape as well as associated pile-up dopant profile are prone to variation, especially for not self-aligned gate device fabrication. Also, long-channel ultra thin silicon body device simulations require a detailed simulation mesh resulting in extensive computational effort. Therefore, only a not strictly physically motivated calibration at a single operation point against device characteristics at controlled 323 K is presented here. Note, the simulation results do not claim any absolute accuracy but are mainly introduced to illustrate physical aspects and to derive general trends for future fully self-aligned DeFET device optimization.

The Synopsys TCAD simulation setup comprises the *Synopsys Device* default model for drift-diffusion (DD) based carrier transport [23, pp.184] based on Fermi charge carrier distribution statistics [23, pp.178]. The carrier mobility is modeled with the defaults for doping and temperature dependence [23, pp.321]. Besides the default bandgap narrowing model [23, pp.251], Schockley-Read-Hall recombination depending on doping and temperature as well as electric field (Schenk model) are included [23, pp.395]. Further, a model for the lattice temperature [23, p.185] and for non-local tunneling at the metal-to-semiconductor interfaces [23, pp.733] including non-simplified Schottky barrier lowering (SBL) for thermal emission (TE) and approximated SBL for field emission (FE) are part of the TCAD simulation setup [23, pp.210][21,

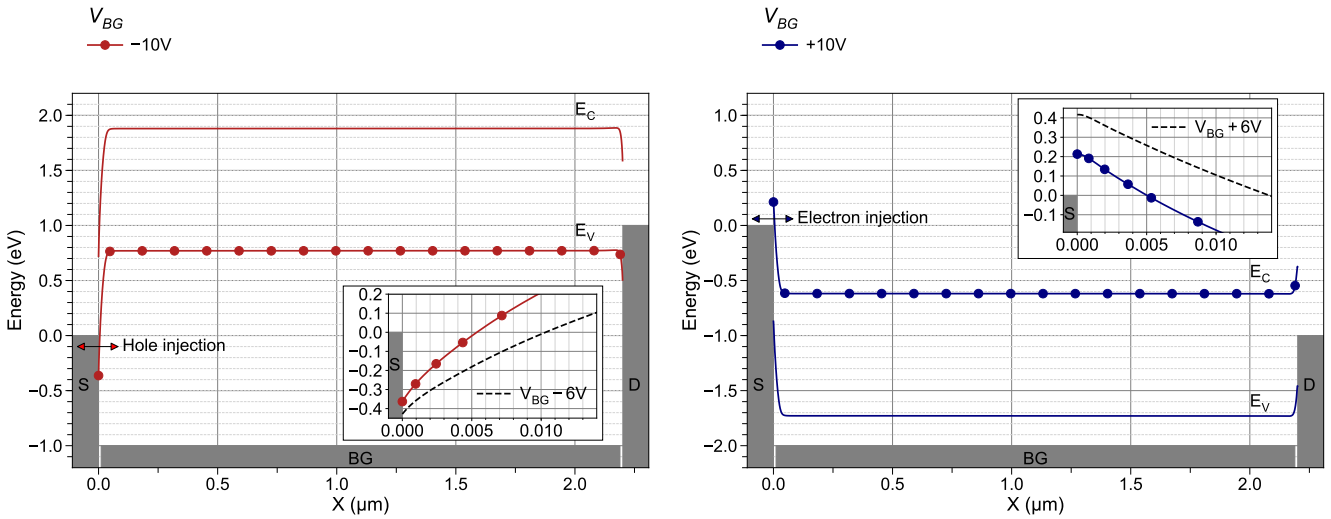
22]. Quantum effects are not included as the silicon body thicknesses t_B of >7 nm are comparatively large and the influence of quantum confinement is therefore in the context of this work negligible [120, 121].

Due to convergency issues of the Schrödinger SB tunneling model, the more stable but less physically accurate nevertheless commonly used Wentzel-Kramers-Brillouin (WKB) tunneling approximation model [23, pp.741] in conjunction with Schottky barrier lowering (SBL) is implemented for the here following simulations. In order to partly compensate for the inherent overestimation of tunneling current by the WKB model, the tunneling masses for holes and electrons are adjusted to $0.42\,m_0$ and $0.41\,m_0$, respectively, following the approach of R. Vega in order to realize a fit in the more relevant $I_{DS,on}$ region [122, pp.13][123–125]. The effective Richardson's constants for holes and electrons are defined to silicon standard values of 32 and 112 A/cm^2K^2 [122]. Still, an overestimation for high $I_{DS,on}$ regimes by the WKB approximation is observed due to the WKB wide barrier assumption being violated by the thinned SB widths and the contribution of SBL in pronounced transistor on-state regimes [123]. Also, high-field carrier velocity saturation and thin film carrier mobility degradation models are not included for convergency reasons which further contributes to the excess of $I_{DS,on}$ current [19, pp.316]. In order to compensate for this overestimation a lumped S/D resistance [23, pp.215] is introduced as an additional fitting parameter for the SB resistance resulting in good agreement of simulation and experimental data for $I_{DS,on} > 100\,nA/\mu m$ as illustrated in Fig. 25a. This approach is favored over neglecting SBL or thermionic emission (TE) contribution as proposed by R. Vega [20]. A more sophisticated yet not fully self-consistent approach based on a proprietary simulator extension is given by Padilla et al. [25].

Based on the simulation, the carrier injection at the source contact is illustrated in the band diagrams in Fig. 27 (insets) for hole and electron conduction. For $V_{BG} = -10\,V$ the SBL effect reduces the barrier height from initially 0.4 to 0.35 eV and reduces the tunneling distance at 0 eV to 5 nm. Note, that the commercial simulator does not present the band diagrams with the full SBL band shaping effect used internally for the calculation of the FE contribution and only includes the SBL correction factor for the SB height for the TE contribution in the here depicted band diagrams [22].

In contrast to the BG, the FG transistor resembles a depletion mode or normally-on FET. The FG electrode locally, i.e. in the region underneath the FG electrode, affects the channel of the BG transistor and therefore controls the charge carrier flow between source and drain.

To obtain the intended operation of the dehancement mode RFET, an operating point has to be set by a DC voltage biasing of the BG electrode. This operating point determines the threshold voltage, maximum $I_{DS,on}$ current and the dominant charge carrier type. The actual switching behavior and control of $I_{DS,off}$ is realized by applying a voltage to the FG with a sufficiently



(a) PMOS biasing, $V_{DS} = -1$ V, $V_{BG} = -10$ V

(b) NMOS biasing, $V_{DS} = +1$ V, $V_{BG} = +10$ V

Fig. 27: Simulated long-channel device band diagrams parallel to the body to-BOX interface at 1 nm inside the Si-body layer at 323 K (compare Fig. 28). Insets illustrate source contact in detail.

high opposite polarity with respect to the BG potential. The resulting operation modes are summarized in Table 2.

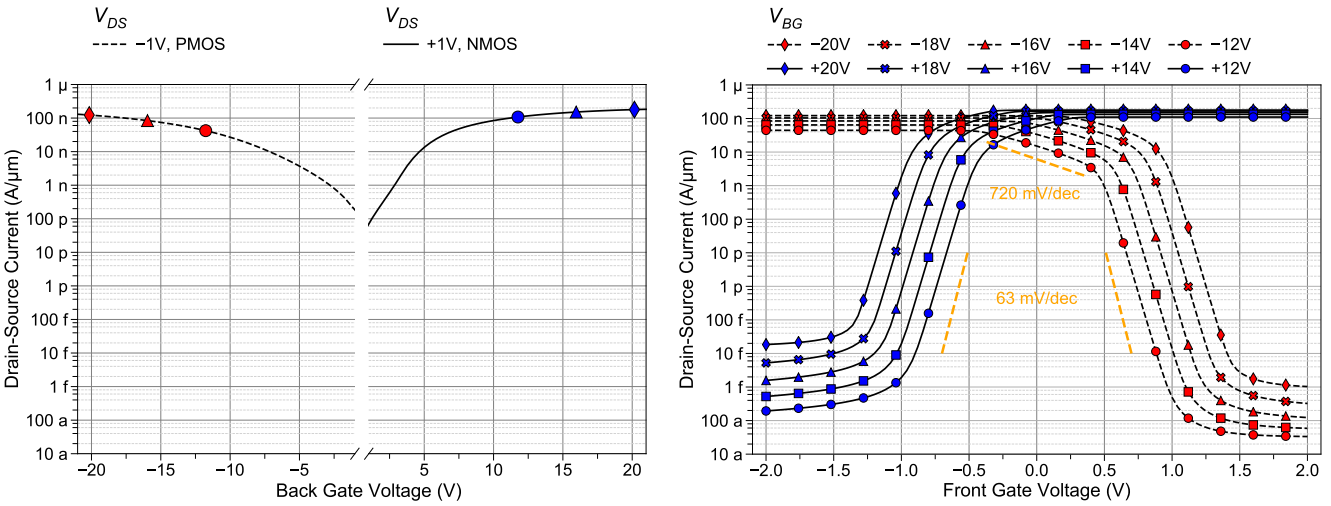
Biasing	$V_{BG} \gg 0$ V (NMOS)	$V_{BG} \ll 0$ V (PMOS)
$V_{FG} \gg 0$ V	Conducting / on-state	Channel locally depleted / off-state
$V_{FG} \ll 0$ V	Channel locally depleted / off-state	Conducting / on-state

Tab. 2: Dehancement mode operation states.

The simulated FG input characteristics for NMOS and PMOS operation are illustrated in Fig. 28b. The $I_{DS,on}$ current as well as the threshold voltage (V_{th}) are depending on the magnitude of V_{BG}. By biasing the $V_{BG} \gg 0$ V ($V_{BG} \ll 0$ V) unipolar NMOS (PMOS) behavior is predicted by the simulation while the sub-V_{th} slope reaches almost the theoretical limit with 65 mV/dec for both types. As a result of the depleting effect of the FG on the BG channel a theoretical I_{DS} on-to-off current ratio of ~9 decades is achieved (neglecting gate leakage currents). The local depletion of charge carriers below the FG electrode and the buried channel formation at the body-to-box interface are illustrated in Fig. 29 for NMOS operation ($V_{BG} = +12$ V).

The maximum $I_{DS,on}$ current is set by the electrostatic influence of the BG on the SB contacts (compare makers in Fig. 28a with Fig. 28b). For instance, biasing the BG at $V_{BG} = -16$ V for $V_{DS} = -1$ V results in a PMOS $I_{DS,on}$ current of $I_{DS,on} = 80$ nA/µm (red triangles). As discussed in more detail in the next section, contrary to classic p-n junction based MOSFET, the SB resistance of mid-gap SB contacts, i.e. the junction resistance, dominates the total transistor resistance for moderate V_{BG} magnitudes. The SB resistance leads to a distortion of the PMOS linearity for $V_{BG} < -12$ V. As the BG potential is not sufficient to achieve transparent hole injection, the I_{DS} current slope is limited to 720 mV/dec for -0.4 V $> V_{FG} <$ 0.4 V (Fig. 28b). Decreasing the FG

potential from 0.6 V to 0.4 V results in a decreased potential barrier for holes and consequently a decreasing V_{DS} potential drop over the FG depletion region. Hence, the V_{DS} potential drop over the SB resistance commences to dominate the total transistor resistance in the transition from the sub-V_{th} to the on-state region. This simulation result is supported by the experimental FG input characteristics illustrated in Fig. 32 exhibiting similarly limited I_{DS} current slopes in the linear region.



(a) BG input characteristics

(b) FG input characteristics for referenced V_{BG} biasing

Fig. 28: Simulated long-channel DeFET device input characteristics at 323 K.

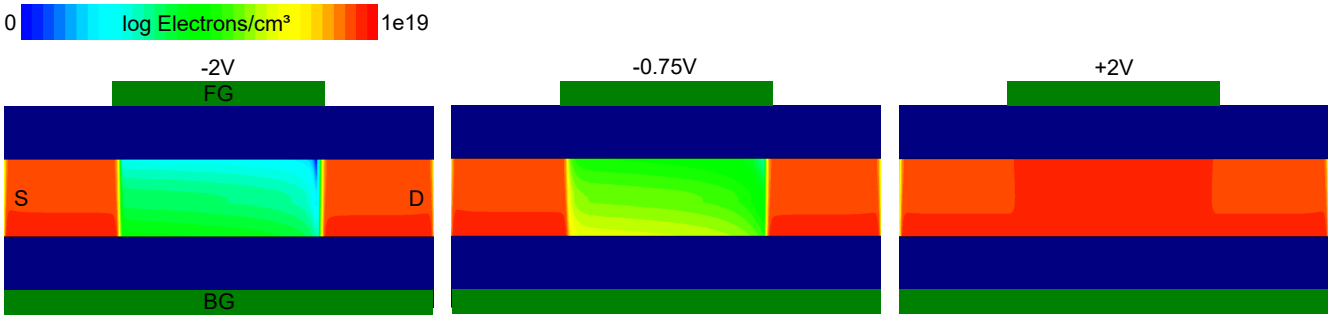
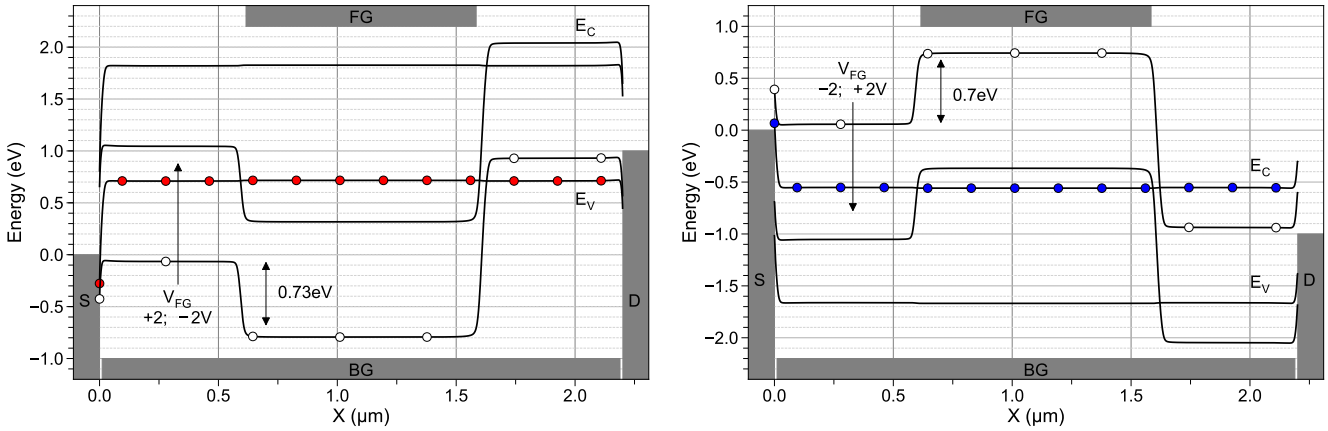


Fig. 29: Schematic illustration of electron channel depletion. V_{DS} = +1 V, V_{BG} = +12 V at 323 K (not to scale).

A remarkable feature of the DeFET is the low off-state leakage current ($I_{DS,off}$). Experimental devices show $I_{DS,off}$ leakage current levels fA/µm similar to the leakage levels in the simulations (compare Fig. 32a and Fig. 32a,b with Fig. 28b). The low $I_{DS,off}$ current is the consequence of the exceptionally high FG induced potential barrier of 0.7 and 0.73 eV for N- and PMOS operation, respectively, as derived from the simulated band diagrams depicted in Fig. 30. As charge carriers obey the Fermi-Dirac distribution, virtually no charge carriers statistically acquire sufficient energy to surmount this potential barrier at room temperature. Compared to the predecessor nanowire RFET devices of Wessely et al., the planar DeFET features at least an order of magnitude less $I_{DS,off}$ leakage current per µm of channel width [16, pp.90]. This improvement is based on the reduced Si-body thickness of approx. 8–14 nm of the DeFET and

the resulting increased electrostatic coupling of the FG to the planar channel region compared to the nanowire RFET Π-FG cross section of approx. 65x65 nm^2. The dominant contributors to the remaining I_{DS} leakage current are intrinsic charge carrier generation and gate oxide leakage currents in the experimental devices. The low leakage current is further exploited in the later discussed high-temperature operation in subchapter 3.2.3.

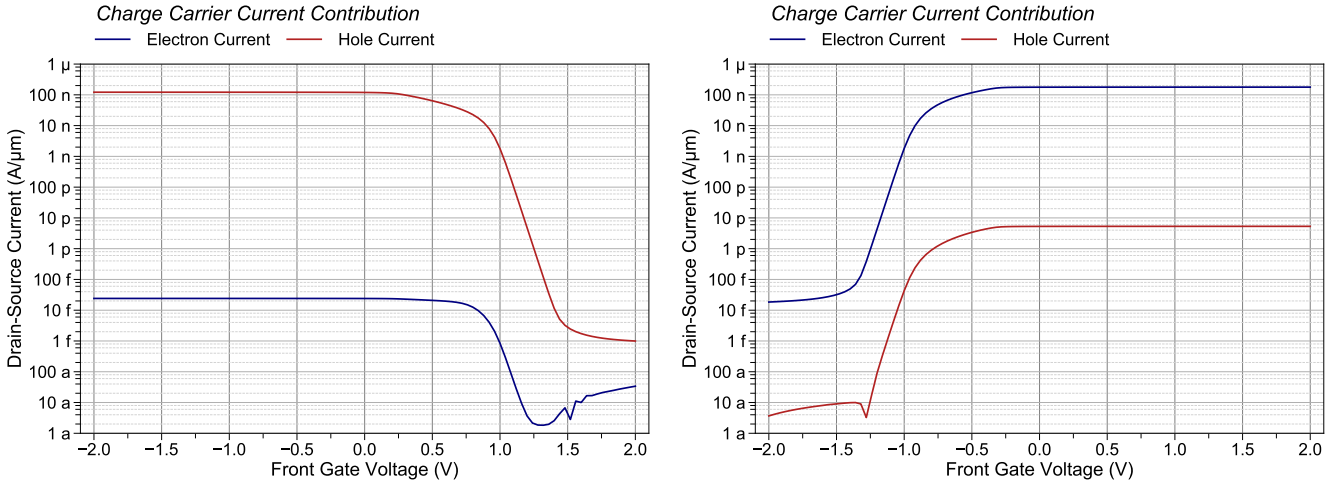


(a) PMOS biasing, $V_{DS} = -1$ V, $V_{BG} = -12$ V

(b) NMOS biasing, $V_{DS} = +1$ V, $V_{BG} = +12$ V

Fig. 30: Simulated long-channel device band diagrams at 323 K.

Another benefit of the splitting of control for the SB carrier injection via the BG and the actual current flow through the device via the FG is the almost complete suppression of the drain side carrier injection normally responsible for ambipolar leakage characteristics and increased $I_{DS,off}$ of SBFET devices. As illustrated in Fig. 31, the FG does not modulate the SB contacts as the electrostatic coupling over 0.6 µm underlap is negligible. This can also be concluded from the perfectly flat valence and conduction bands between S/D and FG over the FG underlap distance in the off-state (Fig. 30).



(a) PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -20$ V

(b) NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +20$ V

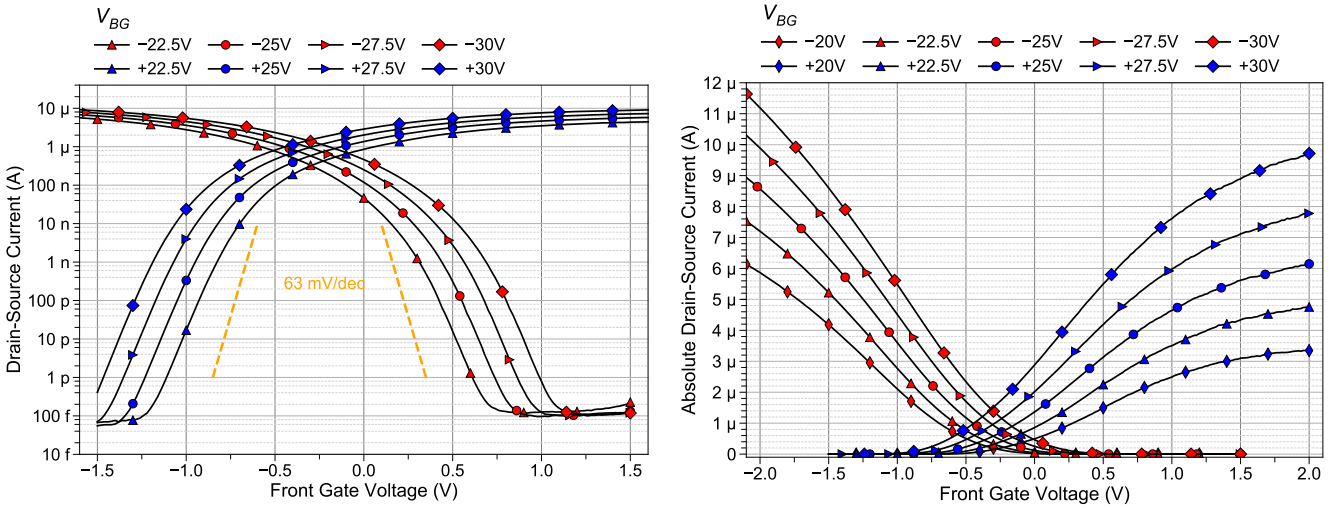
Fig. 31: Charge carrier current contribution to total I_{DS} current for long-channel device.

The experimental POC device input characteristics depicted in Fig. 32 exhibit a comparable behavior with an exceptional I_{DS} on-to-off current ratio of ~8 decades. The sub-V_{th} slope 65–85 mV/dec of the 2nd generation devices is exceptionally close to the ideal simulation results (Fig. 32, Fig. 45, Fig. 50). Similar on-to-off ratios have been obtained from the predecessor nanowire RFET devices although only sub-V_{th} slopes between 89–150 mV/dec could be demonstrated for the nanowire RFET [16, pp.90,p.104]. The I_{DS} on-current for NMOS operation shows a stronger dependency on BG potential comparable to the simulated device (Fig. 28b) indicating similar eSBH properties.

The threshold voltage is shiftable by 75 mV/V_{BG} in the simulation and 70 to 80 mV/V_{BG} in the case of the POC device (Fig. 32). This can be regarded as an indication for correctly derived dielectric thicknesses for the simulation, i.e. FG_{Ox}, Si-body and BOX, as their ratio determines the shiftability.

The measured FG output characteristics depicted in Fig. 34 further demonstrate the electrostatic control of the FG manifesting itself in constant current saturation characteristics. The NMOS biasing exhibits a supra-linear output characteristic at $V_{DS} < 0.7$ V as a typical distortion of SBFET resulting from the threshold of the forward biased SB at the drain limiting charge carrier extraction [108]. On the contrary, the PMOS does not exhibit the distortion as the SB width is electrostatically reduced sufficiently to suppress the drain-side SB diode effect.

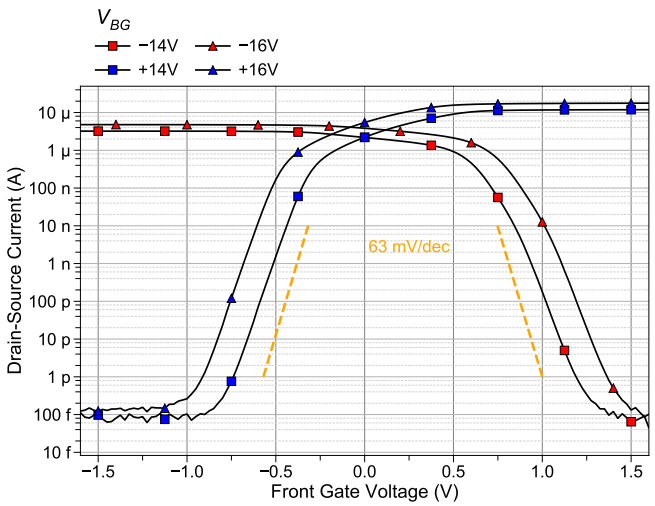
In the next section, a more detailed discussion of the DeFET properties and its suitability for reconfigurable as well as conventional CMOS applications is presented. The foundation for this analysis are parametrized scaled device simulations backed by long-channel POC device characterizations resulting in insights into general trends for a scaled fully self-aligned FG DeFET device design.



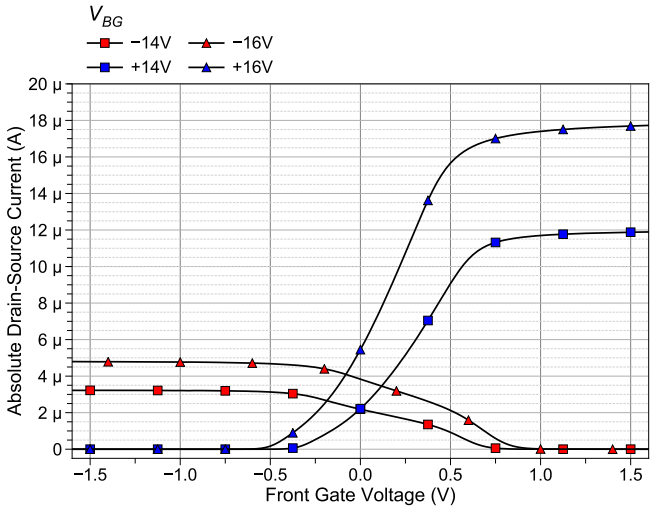
(a) Logarithmic plot, PMOS biasing $V_{DS} = \pm 1$ V

(b) Linear plot, PMOS biasing $V_{DS} = \pm 1$ V

Fig. 33: Input characteristics of Ni metal FG proof-of-concept device, 1st generation (furnace, 300 s). Dimensions: Width 50 µm, BGL 30 µm, FGL 20 µm

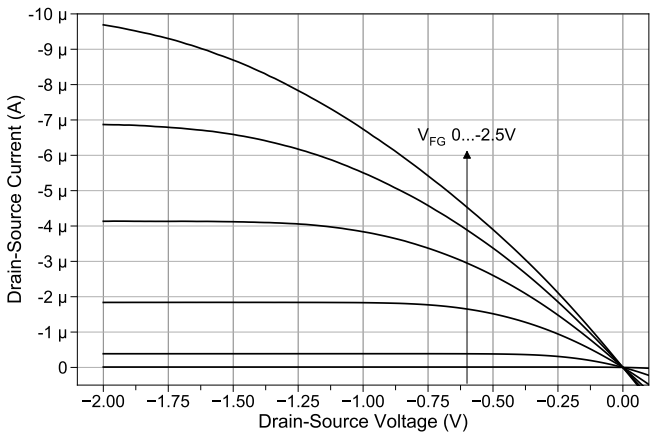


(a) Logarithmic plot, $V_{DS} = \pm 1$ V, respectively

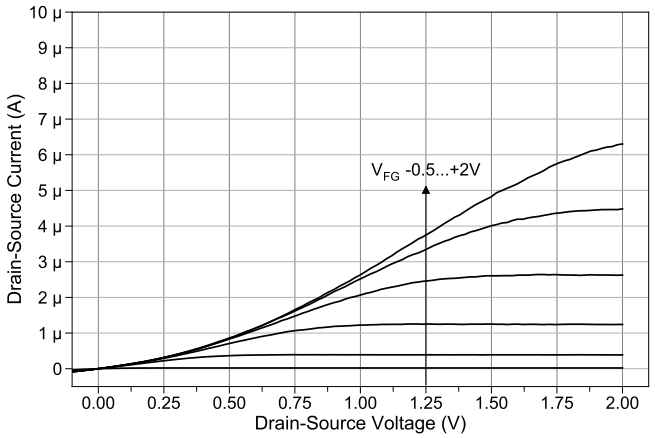


(b) Linear plot, $V_{DS} = \pm 1$ V, respectively

Fig. 32: Input characteristics of $WTiN_x$ metal FG proof-of-concept device, 2nd generation (RTA 60 s). Dimensions: Width 100 µm, BGL 90 µm, FGL 5 µm (compare Fig. 46)



(a) Linear plot, PMOS biasing $V_{BG} = -20$ V, $V_{DS} = -1$ V.



(b) Linear plot, NMOS biasing $V_{BG} = +20$ V, $V_{DS} = +1$ V

Fig. 34: Output characteristics of nickel FG electrode device, 1st generation (furnace, 300 s). Dimensions: Width 50 µm, BGL 30 µm, FGL 20 µm

3.2.2 Experimental and Simulative Design Space Evaluation

In order to further evaluate the DeFET concept, a scaled self-aligned DeFET structure with idealized RFET properties has been selected for the TCAD simulation approach to reduce the computational effort and gain predictive estimates for self-aligned front gate device designs. The idealized RFET properties include symmetric behavior for P- and NMOS operation based on the effect of silicidation induced dopant segregation (SIDS). SIDS is known to be able to adjust the effective SB height (eSBH) in conjunction with NiSi technologies as demonstrated in the following by experimental POC DeFET devices and in the literature [39, 126–128] (see 2.2.2). Another elegant approach to balance the tunneling probabilities for symmetry of an RFET de-

vice is the mechanical strain engineering of the SB contacts as demonstrated successfully by Heinzig et al. and investigated by T. Baldauf et al. [109, 129]. Besides the required symmetry for reconfigurability, a reasonable drive-current ($I_{\mathrm{DS,Drive}}$), CMOS off-current ($I_{\mathrm{DS,CMOS-Off}}$) and transconductance (G_{m}) are required for proper circuit design (see 2.3.3). Also, a co-integration into conventional CMOS topologies based on *hard-wired*, i.e. not reconfigurable, but optimized DeFET devices is considered as well in order to evaluate the feasibility to implement this RFET concept side by side with standard CMOS circuitry in one process technology.

The simulated design of experiments is based on a reference structure depicted in Fig. 35 with the reference design parameters listed in Table 3. As an additional reference for the scaled device simulations, the DD carrier transport model is substituted for the more physically founded hydrodynamic[a] (HD) carrier transport model [130]. In contrast to the DD model the HD model takes the performance diminishing short-channel effects (SCE) into account by additionally considering the actual carrier energy [23, pp.197]. But, the higher computational effort paired with convergency issues impede its general use in this experimentally orientated thesis.

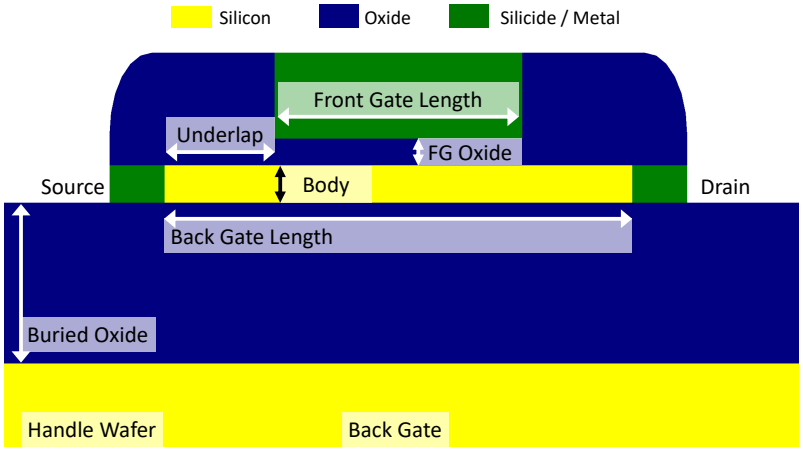


Fig. 35: Scaled dual-gate DeFET simulation reference structure.

Parameter	Unit	Design range	Reference	Figure
FG oxide thickness	nm (EOT)	1, 2, 3	1	Fig. 39
Body layer thickness	nm	5, 7, 9, 12, 15	7	Fig. 39
Buried oxide thickness	nm	30		
FG length	nm	30, 60, 90, 120, 150	90	Fig. 41
FG underlap	nm	20, 30, 40, 50	40	Fig. 43
FG work function	eV	4.38, 4.68, 4.98	4.68	Fig. 44
SB height for electrons (ϕ_{Bn})	eV	0.63, 0.1, 1.0	0.63	Fig. 53
Tunneling masses m^*_{tn} / m^*_{tp}	m_0	0.19 / 0.16		

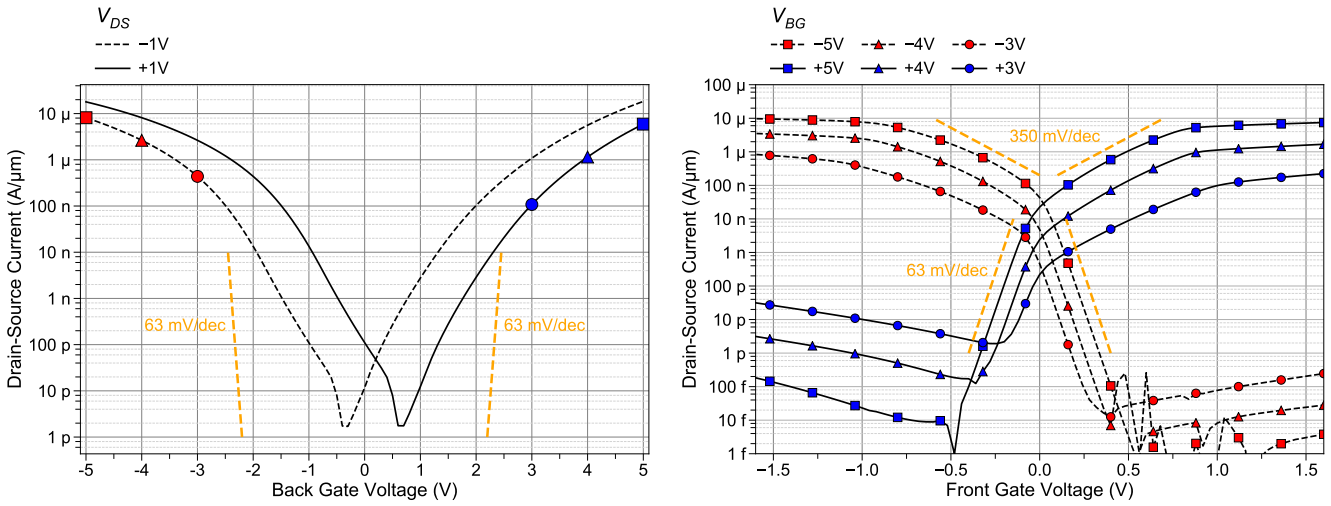
Tab. 3: Design of experiments of device parameter variation.

[a] HD simulation results are diagrammed by green dashed lines.

The simulated reference device features similar BG input characteristics (Fig. 36a) as the experimental POC long-channel devices (Fig. 25a) and corresponds with reported NiSi S/D single-gated SBFET behavior [39, p.14],[126–128, 131].

In contrast to the experimental and simulated long-channel devices, the scaled DeFET exhibits an $I_{DS,off}$ current with an inverse relation to the V_{BG} magnitude (Fig. 36b). This results in a stronger exponential dependence of the maximum I_{DS} on-to-off current ratio on V_{BG} (Fig. 37b). As well, the ambipolarity caused by the drain-side minority carrier injection is more pronounced as illustrated in Fig. 38. Both observations are attributed to the significantly reduced underlap between S/D and FG in comparison to the long-channel devices as is to be discussed in the next section.

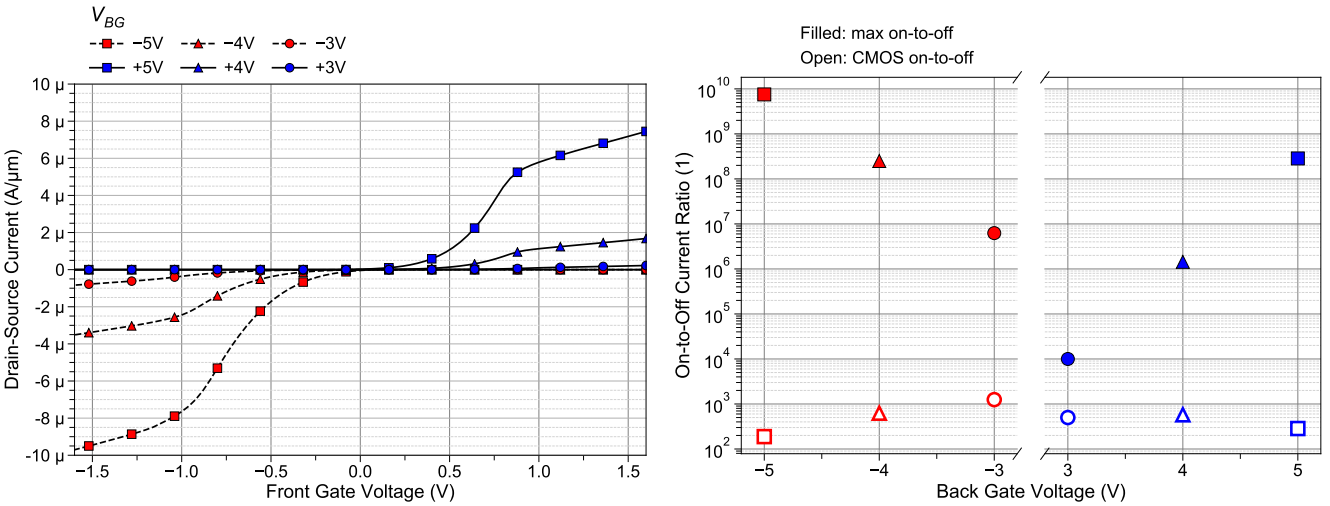
As for the long-channel DeFET, the CMOS I_{DS} off-current ($I_{DS,CMOS-Off}$) depends on the magnitude of V_{BG} (Fig. 36b). Low $I_{DS,CMOS-Off}$ leakage currents for P- and NMOS operation between 300 pA/µm and 30 nA/µm are obtained for ±3 to ±5 V BG potential although the drive current ($I_{DS,Drive}$) is always over one decade below par compared to conventional scaled FDSOI MOSFET [15, Fig.5]. This results in only approximately 2.5 decades of on/off$_{CMOS}$ current ratio for low BG potentials and even less for increased V_{BG} as illustrated in Fig. 37b. Similar to the long-channel devices, the deep sub-V_{th} region is not reached for $V_{FG} = 0$ V due to the mid-gap work function of the FG not being optimized for separate P- and NMOS operation as it is normally the case for conventional MOSFET technologies. Further, the mid-gap SB resistance reduces the slope to 350 mV/dec in the vicinity of V_{th} (see discussion on Fig. 53). These shortcomings are addressed in detail in the following sections.



(a) BG input characteristic with marked biasing points

(b) FG input characteristic for referenced V_{BG} biasing

Fig. 36: BG and FG input characteristics of reference device.



(a) FG input characteristic, linear plot. PMOS biasing $V_{DS} = -1$ V, NMOS biasing $V_{DS} = +1$ V.

(b) Maximum I_{DS} on-to-off current ratio (filled symbols) and on/off$_{CMOS}$ (open symbols) for different BG potentials.

Fig. 37: FG input characteristics and on-to-off ratios of reference device.

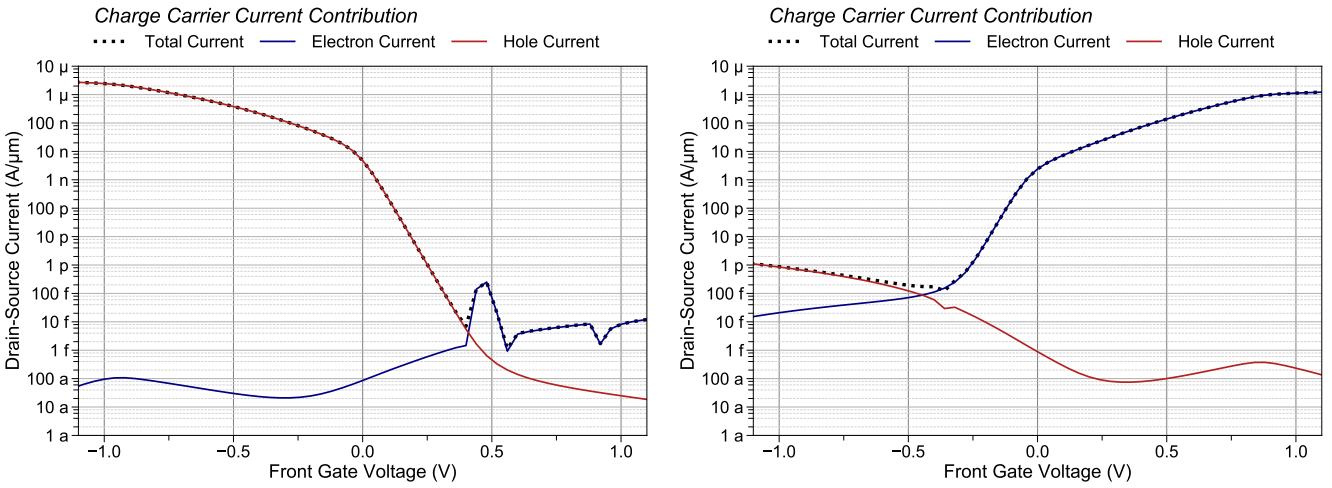
Front- and Back-Gate Engineering

In this subchapter, the discussion commences with the scaling properties of the DeFET. In general, a reduction of the gate length requires an increased electrostatic control of the channel to maintain MOSFET performance, e.g. sub-V_{th} slope, $I_{DS,CMOS-Off}$ and $I_{DS,off}$. Therefore, the influence of the dielectric gate stack on the FG input characteristics is briefly discussed. Thereafter, more DeFET specific design considerations are presented, e.g. the effect of FG length (FGL), FG underlap and FG work function.

The electrostatic control of the FG on the BG induced channel under standard biasing conditions, i.e. moderate V_{DS} biasing without impact ionization, is directly correlated to the threshold voltage (V_{th}) and magnitude of $I_{DS,off}$ leakage current. As common for MOSFET devices, the control of the gate is inversely related to the effective dielectric stack thickness between the gate electrode and the channel and to the effective gate length.

The FG dielectric stack is composed of the FG oxide (FG_{Ox}) and partly the body silicon thickness as the main part of the channel is located at the BOX-to-body interface forming a *buried* channel. For easier comparison of dielectric material thicknesses with different relative permittivities κ_D, the thickness is denoted in units of nm of equivalent (silicon) oxide thickness (EOT) [132].

$$EOT = \kappa_D \cdot \frac{T_{Ox}}{\kappa_{SiO_2}}$$

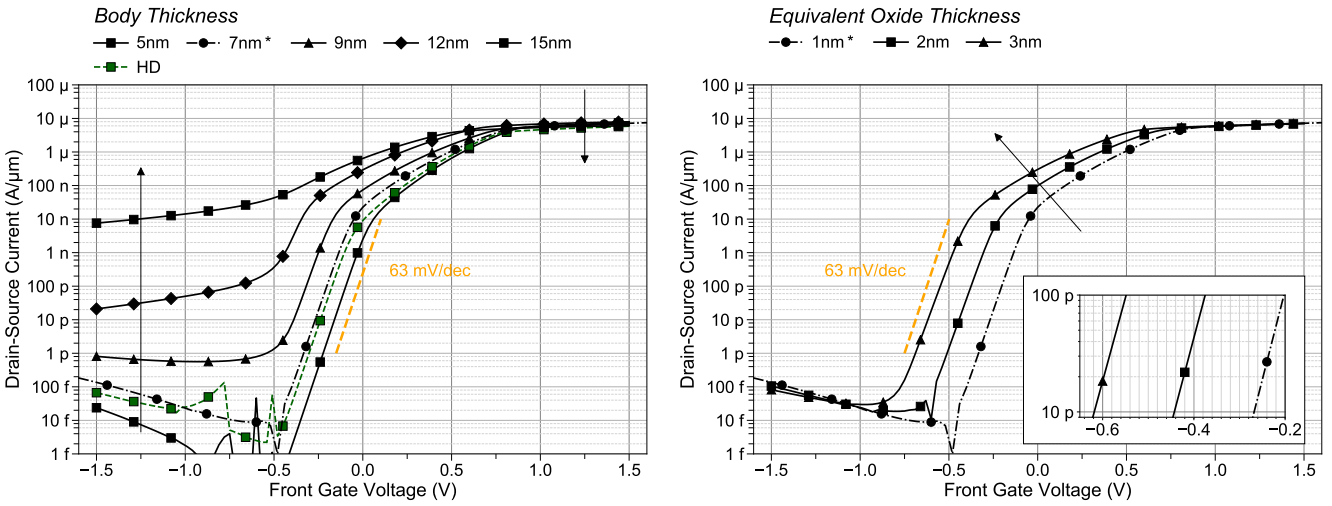


(a) PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -4$ V

(b) NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +4$ V

Fig. 38: Charge carrier current contribution to FG input characteristic total I_{DS} current.

Neglecting quantum capacitance effects the maximum charge carrier density of the channel is located directly at the body-to-BOX interface (Fig. 29) [120, 121]. As the Si-body layer has a relative permittivity of $\kappa_S = 11.9$ [17, p.547] every 3.3 nm of body silicon add up to ~1 nm EOT to the total FG dielectric stack thickness. Fig. 39a illustrates the negative impact of increasing body layer thickness for NMOS operation as the electrostatic control of the FG is diminished, i.e. the $I_{DS,off}$ current increases while V_{th} decreases (PMOS follows same trends). Only for a very thin body thickness of 5 nm a sufficiently high on/off$_{CMOS}$ current ratio of ~3 decades and an $I_{DS,CMOS-Off}$ current of 2 nA/µm are predicted by the DD simulation. As to be expected, the HD simulation yields a slightly lower on/off$_{CMOS}$ ratio as the $I_{DS,CMOS-Off}$ current is predictively increased to 10 nA/µm.

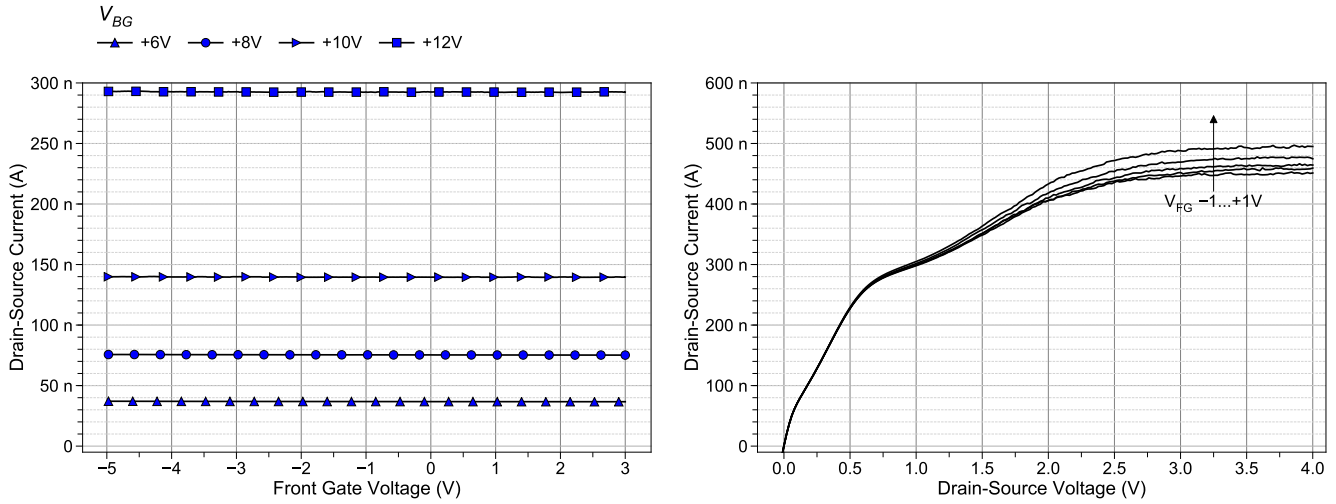


(a) Body thickness influence

(b) FG$_{Ox}$ thickness influence

Fig. 39: Simulated effect of Si-body layer and FG oxide thickness on NMOS FG input characteristics for NMOS operation. PMOS operation follows identical trends. NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +5$ V

Experimentally, this is verified by comparing recessed, i.e. a thinned body layer, (Fig. 32) and not recessed (Fig. 40) DeFET devices with body thicknesses of ~10 and 60 nm, respectively. Note, that the 60 nm body layer results in a partly depleted SOI structure. For the PDSOI device even for very low BG potentials no significant switching behavior can be observed in the FG input characteristic (Fig. 40a). Only for $V_{DS} \gg 1\,V$ a limited influence of V_{FG} is revealed hinting the onset of the formation of a second FG channel segment, i.e. only below the FG, at the surface of the body layer in parallel to the BG channel effectively reducing the total channel resistance (Fig. 40b). Noteworthy, the $I_{DS,on}$ current decreases with increasing body thickness due to the loss of electrostatic control of the BG over the source SB contact reducing the carrier injection efficiency (Fig. 39a) [131]. Similar results have been obtained by F. Wessely for the predecessor nanowire RFET with large channel widths and for NiSi-S/D SOI SBFET devices by J. Knoch et al. [16, pp.99],[131].



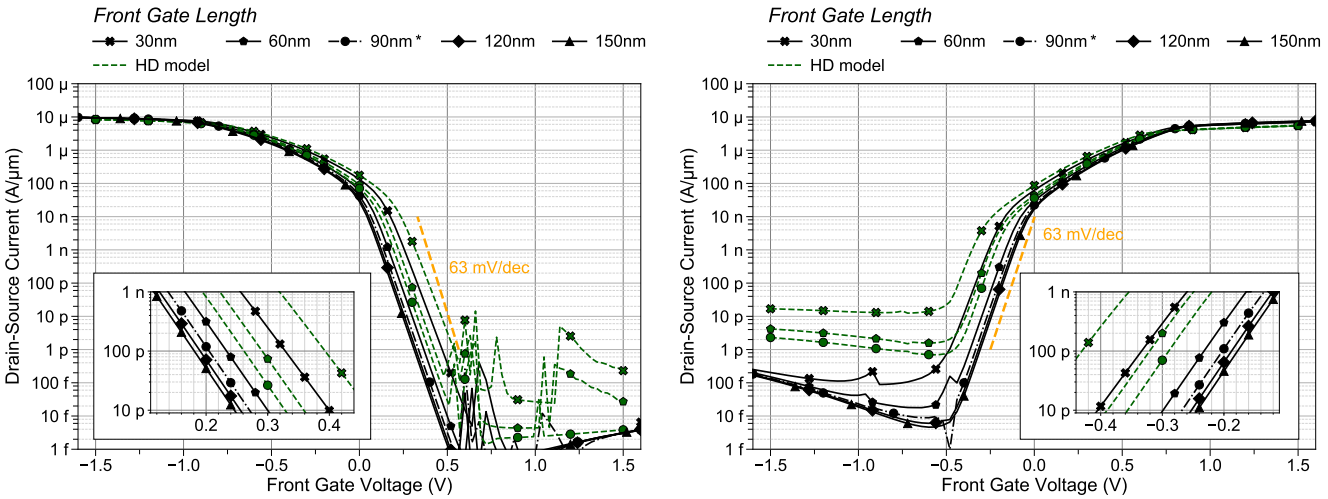
(a) FG input characteristic, NMOS biasing $V_{DS} = +1\,V$ **(b)** FG output characteristic, NMOS biasing $V_{BG} = +12\,V$

Fig. 40: Measured effect of Si-body layer thickness of ~60 nm on FG input and output characteristics.

In contrast to conventional MOSFET, an increase of gate oxide thickness (here FG_{Ox}) does not reduce the $I_{DS,on}$ current as it is determined by the electric field of the BG (Fig. 39b). As the electrostatic control of the FG is reduced, V_{th} is reduced and consequently $I_{DS,CMOS-Off}$ increases. On the other hand, decreasing the BOX thickness increases the electrostatic coupling of the BG to the SB interfaces and channel. This stronger coupling increases $I_{DS,on}$ but also lowers V_{th} for given V_{BG} (not shown here). This effect can also be generated by increasing the BG potential, as the electrical field effect is the driving force. But, given the limited supply voltages in CMOS circuits a reasonably thin BOX has to be selected. Lately, these performance reducing effects of FG_{Ox} and body layer thicknesses have been demonstrated via below par designed RFET devices by Yojo et al. [133].

Peculiarly, the simulated scaling of the FGL from 150 nm down to 30 nm does not lead to a significant increase of sub-V_{th} slope and $I_{DS,off}$ current as illustrated in Fig. 41. For N- and

PMOS biasing, the sub-V_{th} slopes theoretically remain close to the ideal limit of 63 mV/dec at 300 K. Based on HD simulations (green dashed lines), sub-V_{th} slopes of 77 mV/dec for 30 nm and 65 mV/dec for 60 nm FGL devices are predicted. The results correspond well to reported slopes for FDSOI MOSFET technologies as summarized by B. Doris et al. [15].
As to be expected, the comparison of the DD and HD carrier transport model yields the underestimation of SCE of the DD resulting in its overestimation of V_{th} and $I_{DS,on}$ as well as underestimation $I_{DS,off}$. However, given the uncalibrated scaled simulation approach and the objective to derive trends by relative comparison, the DD simulations are considered to be sufficiently precise.



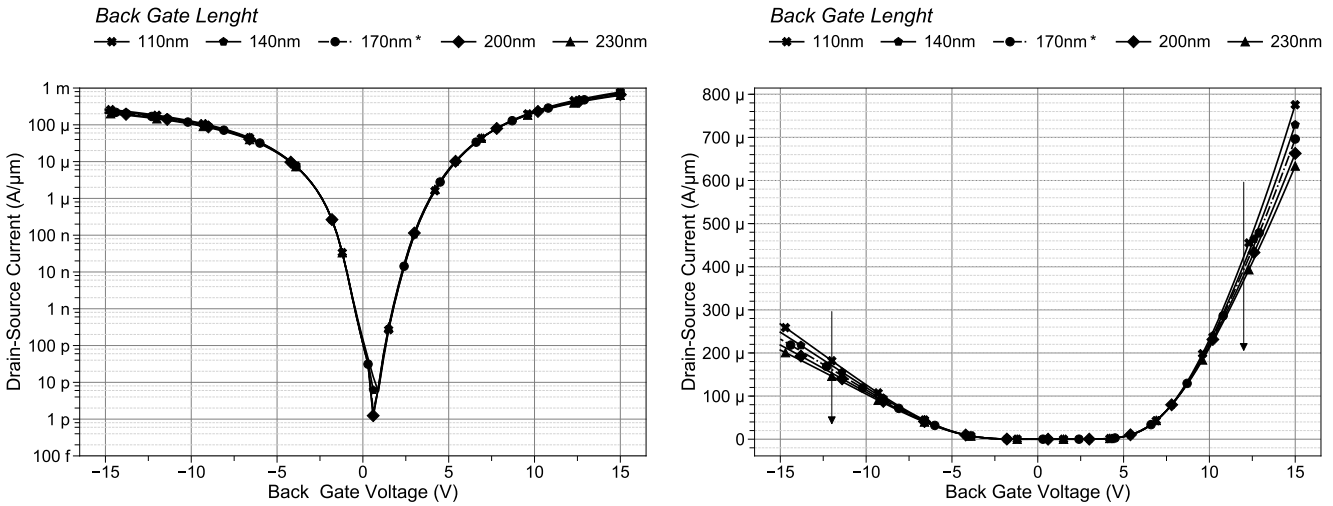
(a) PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -5$ V

(b) NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +5$ V

Fig. 41: Effect of FG length on FG input characteristics.

As the maximum $I_{DS,on}$ is limited by the BG, scaling of the FGL does not increase $I_{DS,on}$ as it is the case for conventional MOSFET devices. Therefore, the scaling effect of the back gate length (BGL) is depicted in Fig. 42. For $-5\,V > V_{BG} < +5\,V$ no scaling effect in terms of $I_{DS,on}$ is observed. Only after increasing the V_{BG} magnitude beyond ±10 V, a theoretical scaling effect is observable. As discussed previously, the injection efficiency of the mid-gap SB is insufficient at low V_{BG} and the SB junction resistance is therefore dominating the scalable channel resistance as it is typical for SBFET with finite barrier heights [17, p.203]. On the other hand, increasing the BG potential decreases the V_{th} and consequently increases $I_{DS,CMOS-Off}$ rendering the device incompatible with CMOS circuit applications. This issue is addressed in the later following subsection on SB engineering.

A specific scaling limit for the dual-gate DeFET is the necessity of an underlap to the S/D SB contacts. As can be derived from Fig. 43, decreasing the underlap distance increases the electrostatic coupling of the FG to the S/D SB contacts. This coupling increases the drain-side minority carrier injection resulting in an increased ambipolar characteristic in form of an increasing $I_{DS,off}$ current. For an underlap of 20 nm the FG commences to dominate the electro-

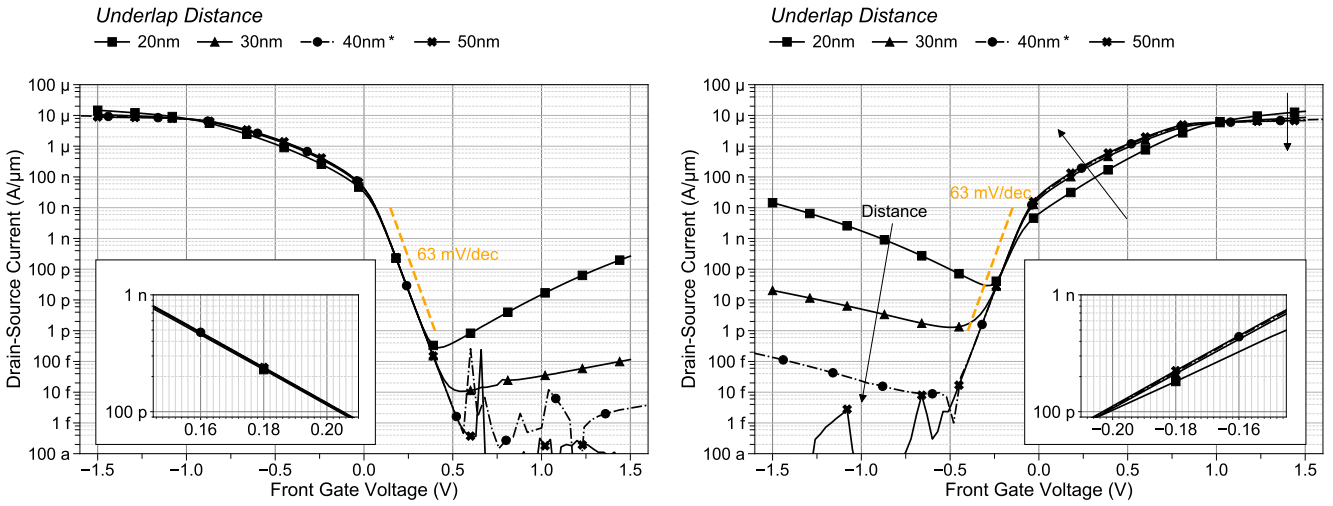


(a) Logarithmic plot

(b) Linear plot

Fig. 42: Effect of BG length on BG input characteristics. $V_{DS} = +1$ V.

statics at the SB contacts illustrated by the onsetting deviation of the FG input characteristics in the on-state, i.e. a lower I_{DS} current for $0 < V_{FG} < 1$ V and higher I_{DS} for $V_{FG} > 1$ V in NMOS operation as depicted in Fig. 43b. Noteably, the increase of I_{DS} is not beneficial for CMOS circuits as the $I_{DS,Drive}$ current for $V_{FG} = V_{DS}$ stays constant.



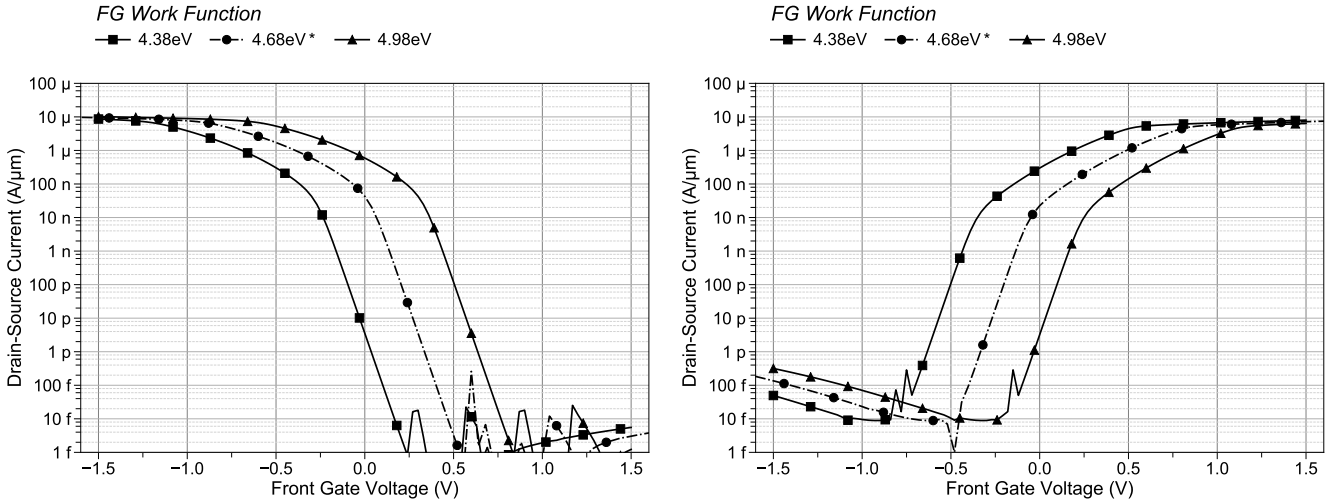
(a) PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -5$ V

(b) NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +5$ V

Fig. 43: Effect of FG underlap on FG input characteristics.

In order to optimize the dual-gate DeFET for CMOS circuits two issues have to be addressed. Firstly, the low $I_{DS,on}$ and secondly, the low V_{th} resulting in significant $I_{DS,CMOS-Off}$ current or static leakage. Both issues are limiting the on/off$_{CMOS}$ ratio to only ~2 decades. Proposals for improving $I_{DS,on}$ will be presented in the later following subchapters on SB engineering and in section 3.2.4 on an optimized device structure. In the following paragraphs, possible optimizations for V_{th} for RFET and conventional CMOS applications are presented.

As stated before, for conventional CMOS transistor designs PMOS and NMOS transistors are independently optimized, amongst others, by work function engineering of the gate electrode [17, p. 192]. Introducing this strategy for simulated DeFET devices by changing the work function of the FG from close to mid-gap 4.68 eV by moderate ±0.3 eV results in a shift of V_{th} by ±0.3 V as can be derived from the sub-V_{th} shifts in Fig. 44. Implementing a 4.38 eV FG electrode for PMOS devices and a 4.98 eV FG electrode for NMOS devices would theoretically reduce the $I_{\mathrm{DS,CMOS-Off}}$ to 4 pA/µm while being technologically feasible as heavily doped polysilicon gate electrodes are adjustable from 4.05 to 5.05 eV [17, p. 169]. Consequently, solid on/off$_{\mathrm{CMOS}}$ ratios of >5 decades can theoretically be realized. Unfortunately, this approach would render the design of reconfigurable circuits impossible. But, as discussed later, high temperature and conventional CMOS circuits could possibly benefit from the co-integration of hard-wired DeFET devices.



(a) PMOS biasing
$V_{\mathrm{DS}} = -1$ V, $V_{\mathrm{BG}} = -5$ V

(b) NMOS biasing
$V_{\mathrm{DS}} = +1$ V, $V_{\mathrm{BG}} = +5$ V

Fig. 44: Effect of FG work function on FG input characteristics.

Experimentally, FG electrodes consisting of aluminum, nickel and WTiN$_{\mathrm{x}}$ have been realized. As the body thickness slightly varies from device to device, a direct V_{th} based work function comparison leads to imprecise results. But, as a unique feature of the DeFET, a consistent work function comparison is achievable by simultaneously considering V_{th} of P- and NMOS operation. For this method, V_{th} is determined as the V_{FG} value at an arbitrary chosen current level in the sub-V_{th} region, i.e. for $I_{\mathrm{DS}} = 100$ pA, for BG potentials of the same magnitude for P- and NMOS operation. Taking the sum of the derived V_{th} of both operation modes results in a qualitative work function estimate with $\sum = 0V$ indicating a mid-gap work function and $\sum < 0\,V$ ($\sum > 0\,V$) a lower (higher) work function appropriate for PMOS (NMOS) operation. As the V_{th} *symmetrically* decreases for P- and NMOS operation with increasing body thickness, the body layer thickness variance is canceled out. But, sub-V_{th} slope distortions caused by oxide bulk

and interface trap states do introduce an error in this estimation. Therefore, unsteady sub-V_{th} slopes deviating from the theoretical limit of 63 mV/dec are to be considered with caution.

The summed up V_{th} values based on the FG input characteristics of devices with FG electrodes consisting of aluminum (Fig. 45a,b), nickel (Fig. 33a,b) and $WTiN_x$ (Fig. 32, Fig. 46) are summarized in Table 4, Table 5 and Table 6, respectively.

I_{DS} threshold	V_{BG}	derived V_{FG}
100 pA	–19 V	0.69 V
100 pA	+19 V	–1.48 V
Fig. 45		$\sum$ –0.79 V

Tab. 4: Aluminum work function estimation taken from Fig. 45.

I_{DS} threshold	V_{BG}	derived V_{FG}
100 pA	–22.5 V	0.42 V
100 pA	+22.5 V	–0.92 V
Fig. 33		$\sum$ –0.5 V

Tab. 5: Nickel work function estimation taken from Fig. 33.

I_{DS} threshold	V_{BG}	derived V_{FG}
100 pA	–16 V	1.12 V
100 pA	+16 V	–1.07 V
Fig. 46		$\sum$ 0.05 V
100 pA	–14 V	1.02 V
100 pA	+14 V	–0.59 V
Fig. 32		$\sum$ 0.43 V

Tab. 6: $WTiN_x$ work function estimation taken from Fig. 32 and Fig. 46.

As to be expected, the comparison yields aluminum (Fig. 45) as the lowest work function material with an estimate of –0.79 V followed by nickel with –0.5 V (Fig. 33). This corresponds well with typical reported values for work functions of Al and Ni on SiO_2 of 4.1 eV and 4.55 eV, respectively [17, p.169][111, 134].

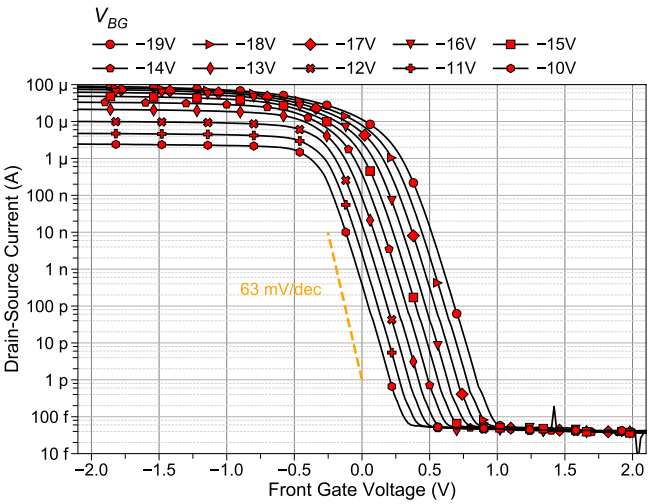
On the contrary, for $WTiN_x$ a significantly higher work function with a span of 0.05 to 0.43 V is estimated (Table 6). The 0.05 V indicate an almost ideal work function for RFET operation close to 4.6 eV mid-gap, although the eSBH for electrons of this device favors NMOS over PMOS operation in terms of $I_{DS,on}$ (Fig. 46). On the other hand, an estimate of 0.43 V is observed as well for an in parallel processed device indicating an even higher work function. This spread is confirmed by further $WTiN_x$ devices (not shown here) hinting at a variability of the reactive

sputter deposition process possibly resulting in different compositions of the $WTiN_x$ material. Based on the respective literature, the composition is suspected to vary greatly between devices as tungsten on SiO_2 is reported with 4.6 eV, while tungsten-nitride (WN) reaches values of up to 5.12 eV and titanium-nitride values of 4.51 eV (TiN) [135–137]. Hence, it is to be suspected for the mid-gap $WTiN_x$ devices, that the Ti share of the WTi 90/10%wt sputter target has predominately reacted to TiN as titanium is known to be a strong gas phase getter material for e.g. nitrogen and oxygen [138, 139]. For the high work function $WTiN_x$ devices, a significant contribution of WN is assumed, resulting in a net increase of the work function. The root cause for this variability is supposedly the location of the gas inlet inside the sputtering deposition process chamber as it is not symmetrically aligned to the sputter target. This likely results in a N_2 concentration gradient in the vicinity of the target and consequently a change in WN to TiN ratio in the ejected particle composition.

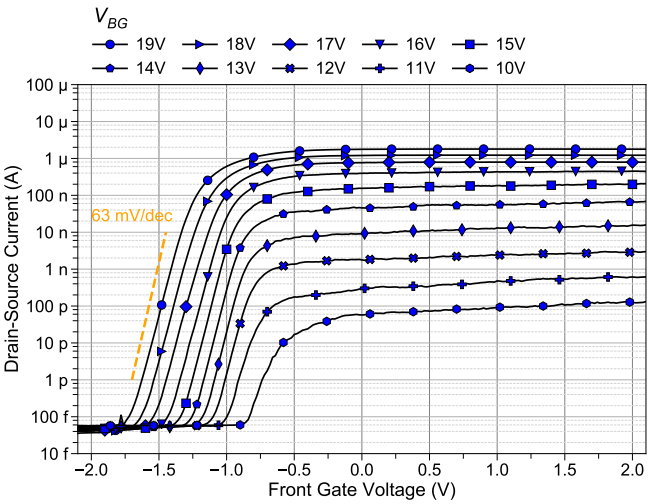
Noteworthy, only for $WTiN_x$ FG electrode devices a hysteresis in the FG input characteristic is observed, exemplary illustrated for NMOS operation in Fig. 46d. The hysteresis is a strong indication for FG_{Ox} trap states in or at the body interface either caused by the high energy sputter deposition process of $WTiN_x$ or by impurities incorporated in the sputter target as the material purity is only 99.9% (3N) in comparison to the electron beam PVD materials with 99.99% (4N). Besides, the DeFET devices have not been finally tempered to reduce oxide trap state densities.

Interestingly, the $WTiN_x$ device FG input characteristics (Fig. 46a,b) correspond exceptionally well with the long-channel device simulations presented previously in Fig. 28. As discussed before, the distortions in the linear region in PMOS operation result from an inefficient hole injection at the source SB.

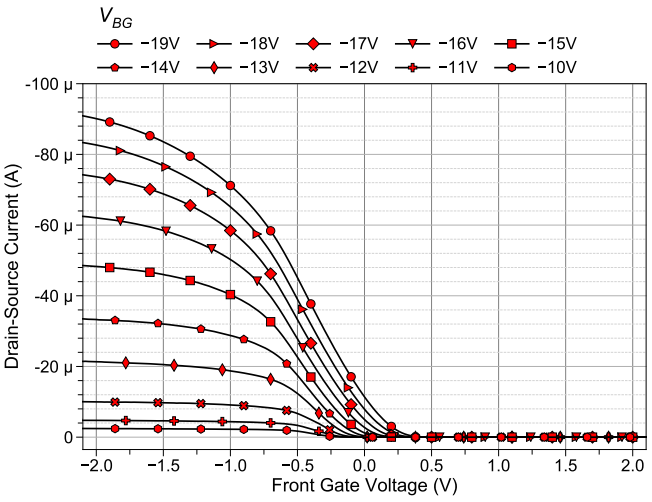
Although, a symmetric FG work function is favorable for CMOS-like RFET circuit designs a sufficiently limited $I_{DS,CMOS-Off}$ and high $I_{DS,Drive}$ are still required for circuit performance.



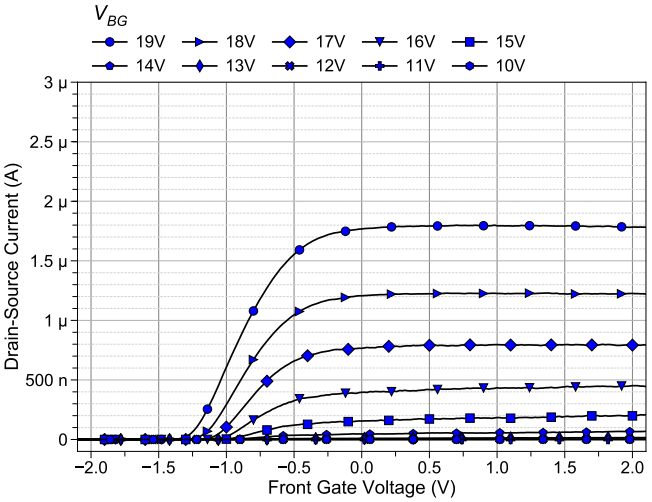
(a) Logarithmic plot, PMOS biasing $V_{\mathrm{DS}} = -1$ V



(b) logarithmic plot, NMOS biasing $V_{\mathrm{DS}} = +1$ V

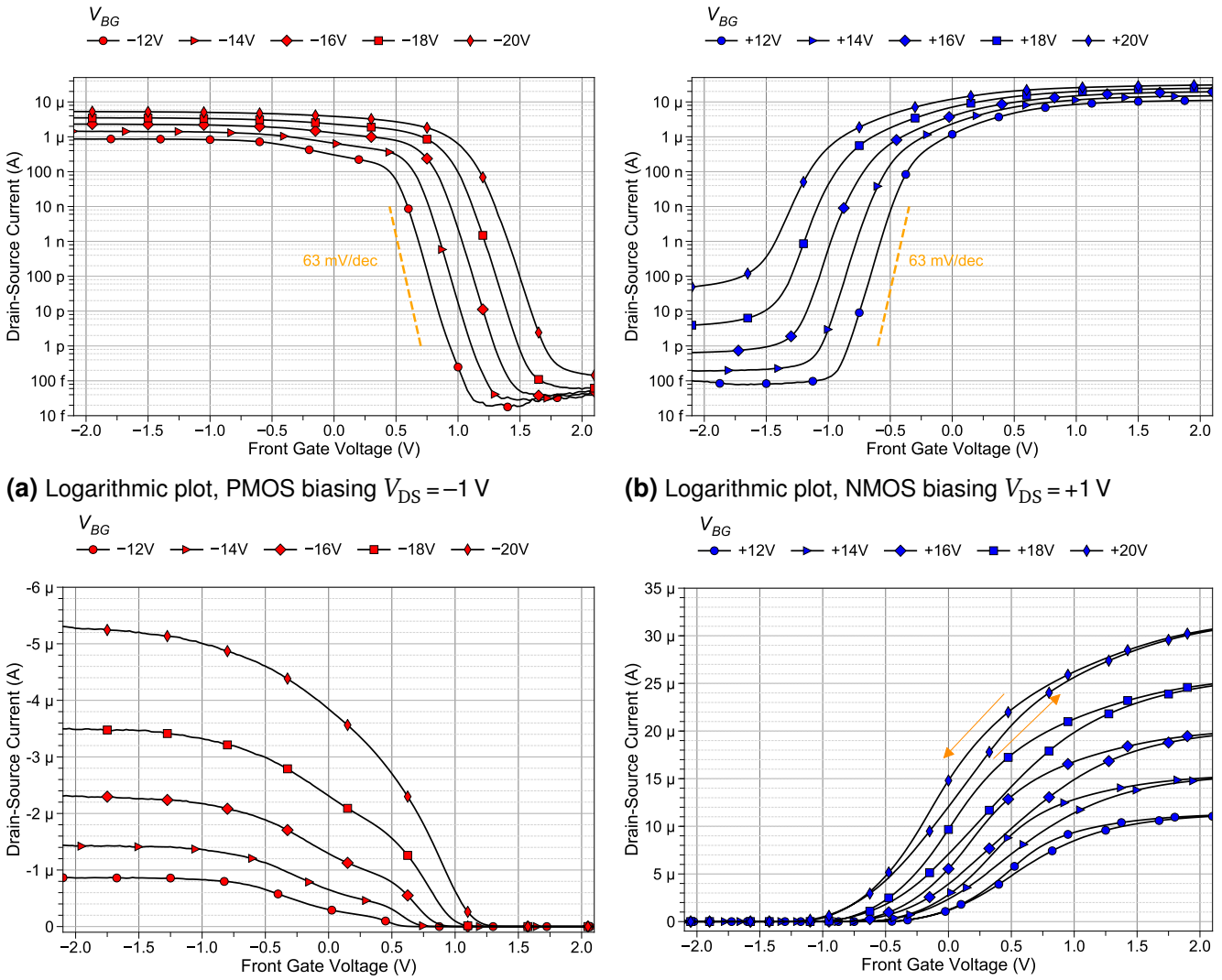


(c) Linear plot, PMOS biasing $V_{\mathrm{DS}} = -1$ V



(d) Linear plot, NMOS biasing $V_{\mathrm{DS}} = +1$ V

Fig. 45: Input characteristics for Al metal FG with NiSi SB, 1st generation (furnace 600 s). Dimensions: Width 50 µm, BGL 30 µm, FGL 10 µm



(a) Logarithmic plot, PMOS biasing $V_{DS} = -1$ V

(b) Logarithmic plot, NMOS biasing $V_{DS} = +1$ V

(c) Linear plot, PMOS biasing $V_{DS} = -1$ V

(d) Linear plot, dual sweep, NMOS biasing $V_{DS} = +1$ V

Fig. 46: FG input characteristics of $WTiN_x$ metal FG device with NiSi SB, 2nd generation (RTA 60 s). Dimensions: Width 100 µm, BGL 100 µm, FGL 70 µm (compare Fig. 32)

In order to further optimize the dual-gate DeFET with regards to $I_{DS,CMOS-Off}$, a dual-metal FG electrode design as depicted in Fig. 47 is experimentally and simulatively evaluated. Essentially, the FG is split into two gates forming a series FG topology between the source and drain terminal with two distinct gate work functions, i.e. 4.38 eV (M1) and 4.98 eV (M2). The simulated FG input characteristic of the dual-metal FG DeFET depicted in Fig. 48 states a significant improvement in terms of $I_{DS,CMOS-Off}$, e.g. $I_{DS,CMOS-Off} = 30\,pA/\mu m$ in comparison to the single-metal FG DeFET $I_{DS,CMOS-Off} = 30\,nA/\mu m$ for $V_{BG} = \pm 5$ V (Fig. 36). As the sub-V_{th} region is reached, > 5 decades of on/off_{CMOS} current ratio and a higher magnitude of V_{BG} leading to an increased $I_{DS,Drive}$ current are theoretically predicted. In this topology, high-performance and low-leakage operation modes with increased $I_{DS,Drive}$ or reduced $I_{DS,CMOS-Off}$, respectively, can be electrically selected by altering the back gate biasing similar to industrial FDSOI MOSFET devices [15, 88]. The energy band diagrams for the dual-metal FG are depicted in Fig. 49 clearly

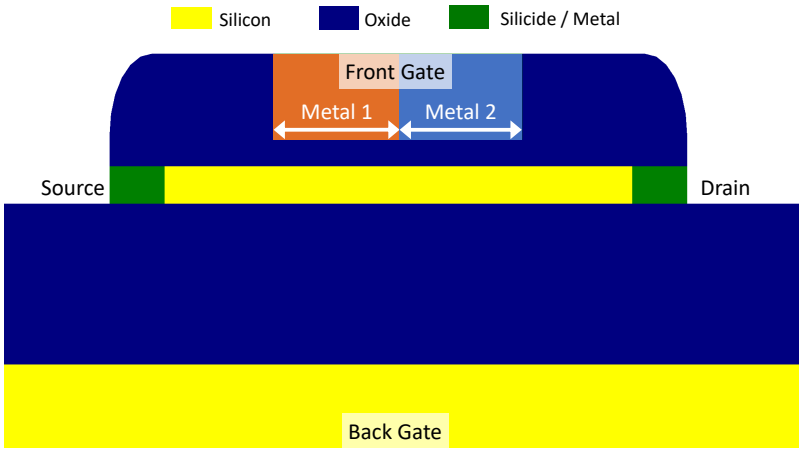
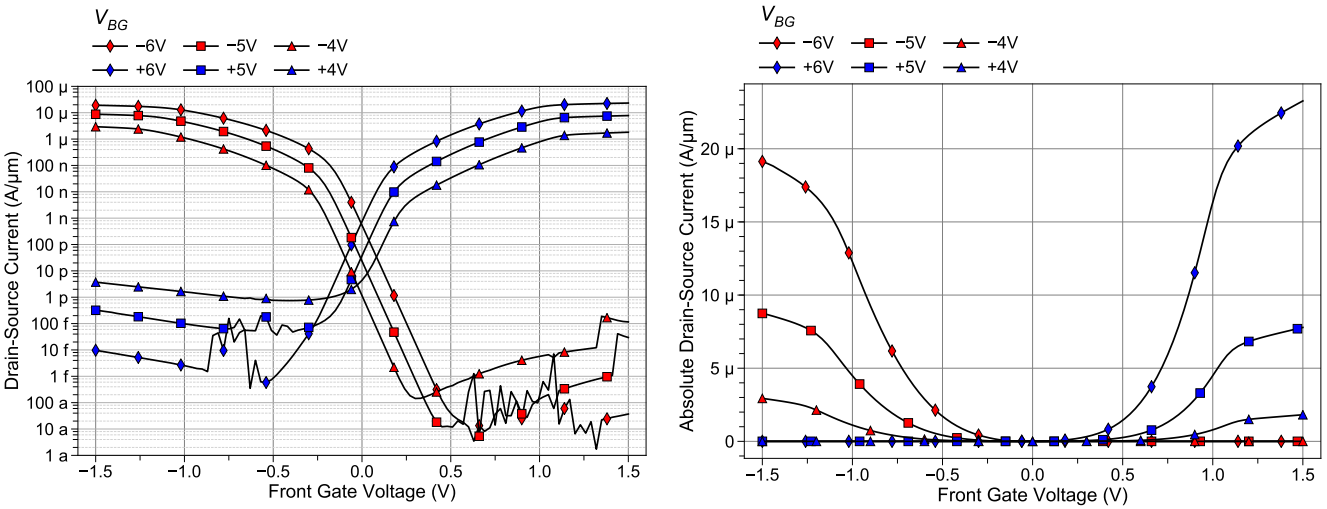


Fig. 47: Dual-metal FG electrode dual-gate DeFET simulation structure.



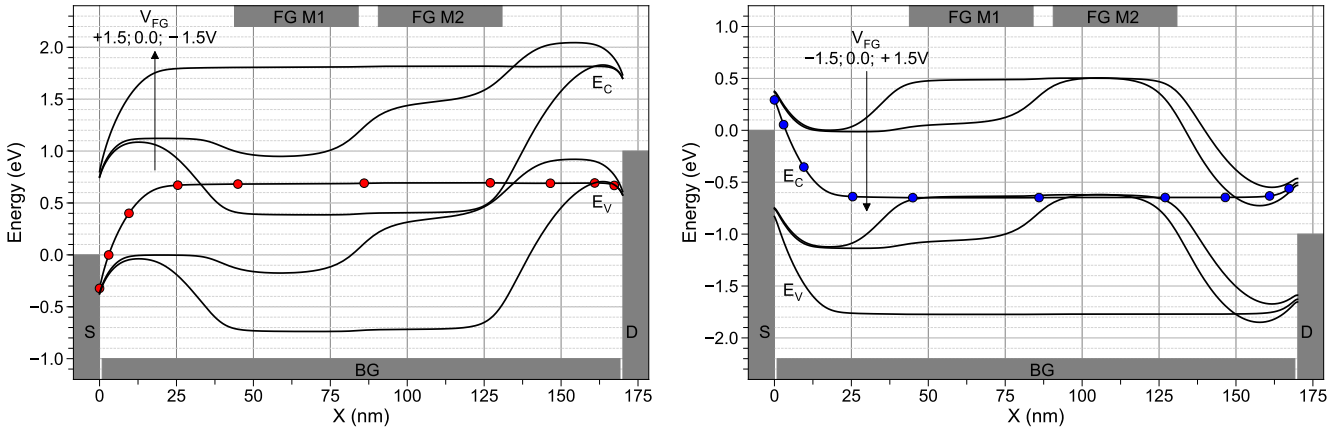
(a) logarithmic plot

(b) linear plot

Fig. 48: Simulated dual-metal FG effect on FG input characteristics, $V_{DS} = \pm 1$ V, FG-M1/M2 4.38/4.98 eV.

illustrating the potential barrier formation of M1 prior to M2 for given FG potential for holes in the valence band in PMOS operation (Fig. 49a) and vice versa M2 prior to M1 for electrons in the conduction band in NMOS operation (Fig. 49b).

Experimentally, dual-metal devices featuring a combined FG electrode consisting of nickel and $WTiN_x$ have been processed as presented in subchapter 3.1 and depicted in Fig. 20b [140]. The FG input characteristic in Fig. 50 exhibits the improved symmetry of the $WTiN_x$ FG between P- and NMOS operation in terms of V_{th}. Closer comparison of V_{th} for $I_{DS} = 100\,pA$ for PMOS operation ($V_{BG} = -12\,V$) yields a threshold increase of 180 mV compared to the single $WTiN_x$ FG device (green curves). For NMOS operation ($V_{BG} = +12\,V$) a slight decrease of 90 mV is measured although the sub-V_{th} slopes differ marginally probably introducing an error into the estimations. As discussed previously, $WTiN_x$ sputter process is suspected to introduce oxide traps although no hysteresis is observed for this device.

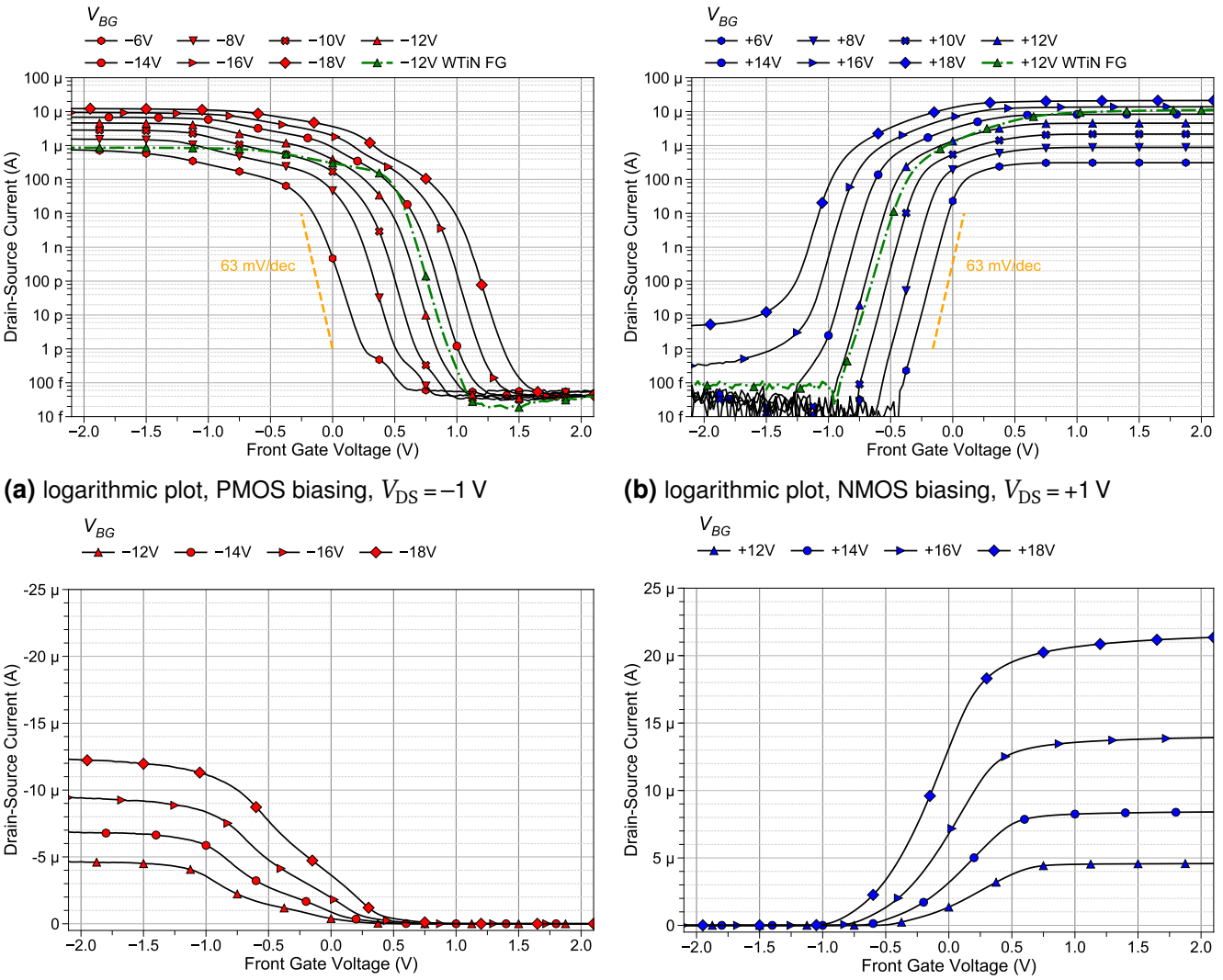


(a) PMOS biasing, $V_{DS} = -1$ V, $V_{BG} = -5$ V

(b) NMOS biasing, $V_{DS} = +1$ V, $V_{BG} = +5$ V

Fig. 49: Dual-metal FG DeFET band diagrams for work function FG-M1 4.38 eV and FG-M2 4.98 eV.

Unfortunately, the experimental devices do not clearly confirm the predicted decrease in $I_{DS,CMOS-Off}$ leakage current. This is owed to the fact, that the work functions of the Ni and $WTiN_x$ FG electrodes do not differ sufficiently compared to the simulated 4.68±0.3 eV work function difference in order to improve the V_{th} for P- and NMOS operation. Also, an interdiffusion of Ni and possibly unreacted Ti during the high energy sputter process is not precluded as both materials exhibit high diffusion rates even at moderate process temperatures [134]. Nevertheless, the general mechanism is regarded to be confirmed cautiously by this experiment. It has to be noted, that a fully self-aligned fabrication approach is assessed to be at least technologically complicated as no straight forward integration of dual work function gates has been reported yet.



(a) logarithmic plot, PMOS biasing, $V_{DS} = -1$ V

(b) logarithmic plot, NMOS biasing, $V_{DS} = +1$ V

(c) linear plot, PMOS biasing, $V_{DS} = -1$ V

(d) linear plot, NMOS biasing, $V_{DS} = +1$ V

Fig. 50: FG Input characteristics for Ni/WTiN$_x$ dual-metal FG, 2nd generation (RTA 120 s). For direct comparison single WTiN$_x$ FG from Fig. 46 (green dashed lines). Dimensions: Width 100 µm, BGL 30 µm, FGL-1 10 µm, FGL-2 10µm

Source/Drain Schottky-Barrier Engineering

In this subsection, an experimentally demonstrated process optimization for increased RFET symmetry in terms of $I_{DS,on}$ for P- and NMOS operation and a simulatively predicted improvement of SB injection efficiency for conventional CMOS applications is discussed.

As presented before, the $I_{DS,on}$ current of the DeFET is mainly limited by the SB charge carrier injection efficiency and less depending on carrier mobilities or gate length. As the doping level of the Si-body is almost intrinsic[a] only the minor surface roughness scattering at the high quality BOX interface in conjunction with the transverse electrical field is degrading carrier

[a] Boron background doping of approx. 1e15 cm^{-3}.

mobilities. Hence, mobilities are considered to be close to ideal values[b] for a MOSFET device [141].

The horizontal furnace based NiSi process, implemented for the 1st generation devices, results in a significantly increased hole conduction branch in relation to the electron branch, e.g. 400 nA/µm for V_{BG} = –15 V and only 800 pA/µm for V_{BG} = +15 V (Fig. 51b, red triangles). As presented in detail in section 2.2.2, this is attributed to a pronounced boron pile-up due to SIDS, which significantly reduces the eSBH for holes. The resulting FG input characteristics of a 1st generation DeFET, depicted in Fig. 45, exhibit an analogous behavior as the predecessor nanowire RFET by F. Wessely et al. although the I_{DS} on-to-off current ratio is comparatively improved to up to 9 decades [16, p.89, Abb. 4.17]. The observed V_{th}-shift and sub-V_{th} slope difference is attributed to the work function difference of the Ni and Al FG electrodes as well as to body and oxide thickness differences between the nanowire RFET and planar DeFET, respectively. In summary, it can be stated that a successful transfer of the furnace silicidation process from the predecessor nanowire RFET to the planar FDSOI DeFET technology has been realized.

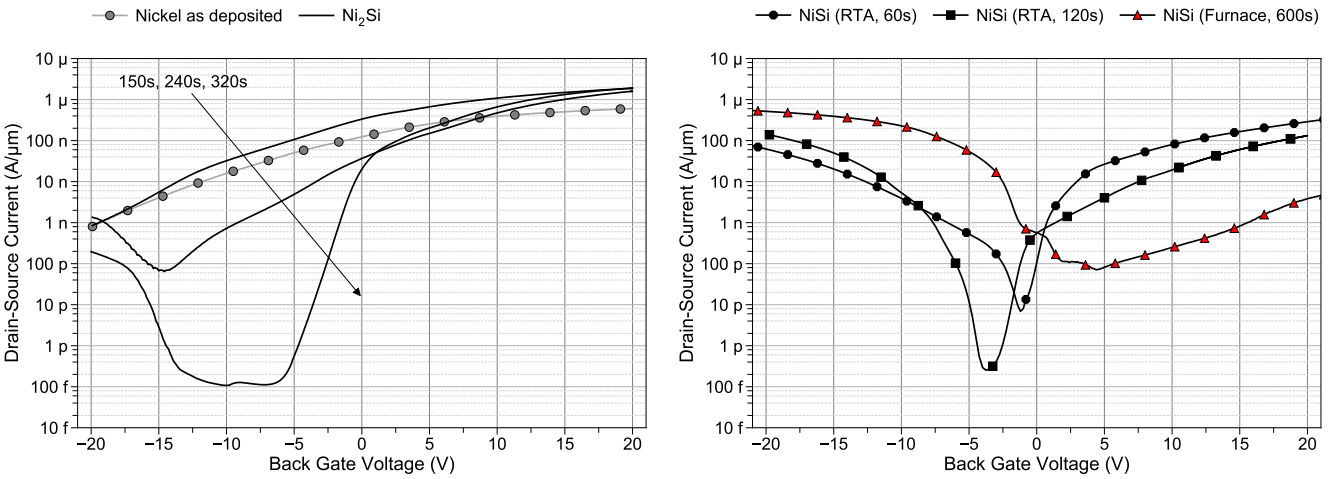
The experimental SB contact formation process of the 2nd generation devices has been controlled via electrical characterization of BG-only (or pseudo) SBFET process monitor devices (see subsection 2.2.3). As the silicidation time of the Ni_2Si soak annealing process increases, an ambipolar characteristic is clearly developing (Fig. 51a).

The second RTA-based silicidation step at 410°C triggers a phase transition of Ni_2Si to NiSi and introduces a boron pile-up due to silicidation induced dopant segregation (SIDS) (Fig. 51b). For an RTA silicidation time of 60 s the eSBH for electrons is lower than for holes as can be derived from the steeper slope and magnitude of I_{DS} in the n-branch (V_{BG} > -2 V) in relation to the p-branch (V_{BG} < -2 V). After additional 60 s (120 s total) of RTA silicidation processing, an almost symmetrical input characteristic in terms of I_{DS} for electron (V_{BG} > 15 V) and hole (V_{BG} < –15 V) conduction is observed. Also, the steeper slope switched to the p-branch for V_{BG} < –4 V clearly indicating a reduced eSBH for holes resulting of the SIDS boron pile up at the NiSi/Si interface. The $I_{DS,on}$ symmetry is also observed for FG input characteristics of 2nd generation devices. As illustrated in Fig. 50c,d a perfect symmetry in terms of $I_{DS,on}$ current of 6.8 and 8.2 µA for V_{BG} = ±14 V is realized.

Based on the experimental results of the 2nd generation RTA silicidation, it is concluded, that $I_{DS,on}$ symmetry for RFET devices is achievable by carefully applying a SIDS SB formation process based on the NiSi silicide technology. Also, low eSBH for holes on p-type silicon are feasible without an additional doping process by utilizing the background doping as the dopant pile-up source.

[b] Bulk mobilities for holes/electrons approximately 505/1450 cm^2/Vs [17, p.547].

The following device simulations are based on the reported capability of NiSi silicide technology to realize < 0.1 eV eSBH for holes and electrons in conjunction with ion implantation and SIDS (see 2.2.2, Fig. 7). The simulated implementation is discussed for hard-wired DeFET configurations for conventional CMOS applications. As the simulation is not calibrated and the WKB tunneling approximation tends to overestimate the I_{DS} current, all results should be assessed with a considerable grain of salt and should be regarded as trends requiring an experimental foundation.

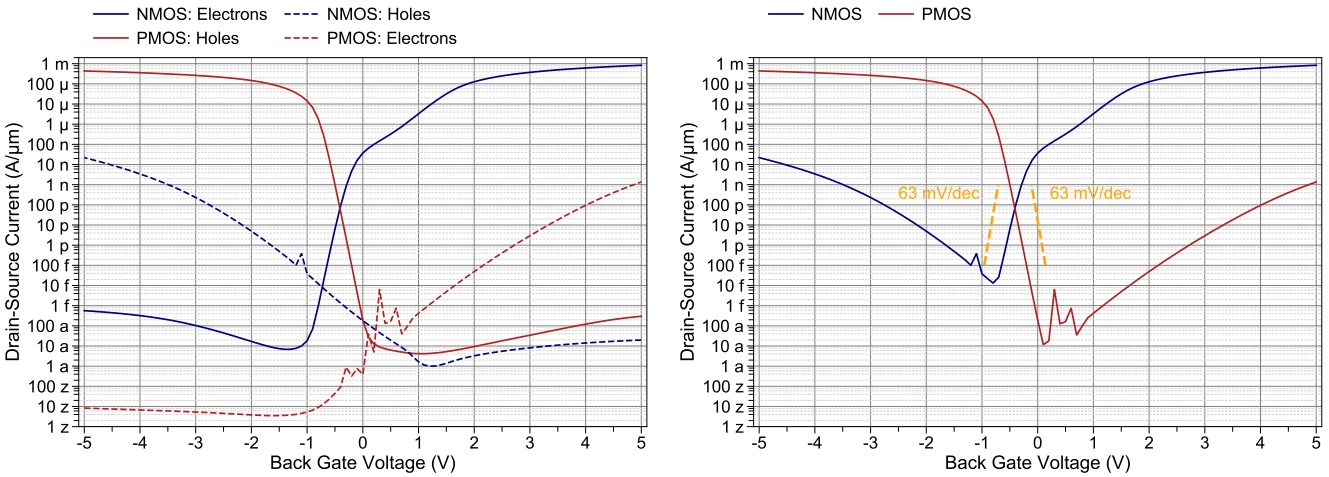


(a) Ni_2Si BG-only SBFET, $V_{DS} = -1$ V **(b)** NiSi BG-only SBFET, $V_{DS} = -1$ V

Fig. 51: BG input characteristics of process monitor devices Ni_2Si and NiSi BG-only SBFET.

As expected, the introduction of a low work function SB for NMOS and high work function for p-type or hole channel MOSFET (PMOS) operation considerably improves the $I_{DS,on}$ current for the preferred carrier type. As illustrated by the BG input characteristics in Fig. 52b, the theoretical implementation increases $I_{DS,on}$ by approximately 2 decades from 8 to 500 µA/µm at $V_{BG} = -5$ V (PMOS operation) and 7 to 900 µA/µm at $V_{BG} = +5$ V (NMOS operation) in comparison to the mid-gap SBH BG input characteristics depicted in Fig. 36a. Also, as the SB resistance is reduced, even the sub-V_{th} slope of the BG input characteristic reaches 66 mV/dec. Further, the ambipolar current is suppressed below 20 nA/µm at $V_{BG} = -5$ V for NMOS and 2 nA/µm at $V_{BG} = +5$ V for PMOS operation (Fig. 52a).

The increased $I_{DS,on}$ for low SBH from the BG input characteristic directly translates to the $I_{DS,on}$ of the FG input characteristics depicted in Fig. 53. For P- and NMOS operation the sub-V_{th}-slope reaches the theoretical limit of 63mV/dec at 300 K and < 1 fA/µm $I_{DS,off}$ confirming the electrostatic control of the FG also in the case of negligible SB resistance. Again, it has to be noted, that the implemented drift-diffusion model underestimates the slope as SCE are not taken fully into account. As the SB resistance is not limiting the I_{DS} current flow, the slope in the transition region between sub-V_{th} and linear region is significantly improved compared to the reference DeFET simulations depicted in Fig. 36b.



(a) Charge carrier current contribution

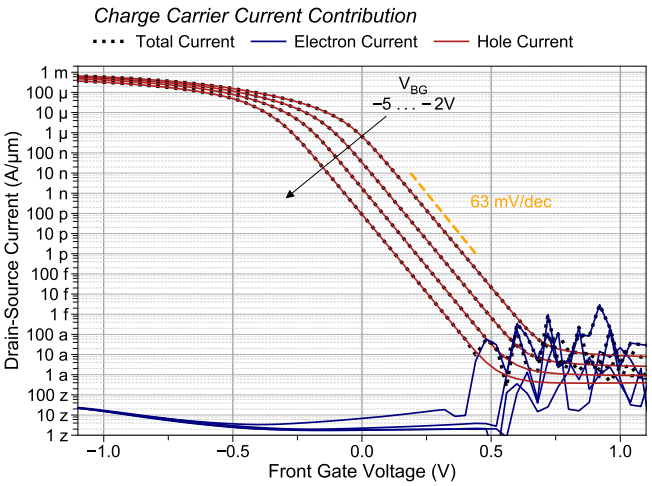
(b) Total I_{DS} current

Fig. 52: Effect of 0.1eV SBH on BG input characteristics.
PMOS $V_{DS} = -1$ V, NMOS $V_{DS} = +1$ V

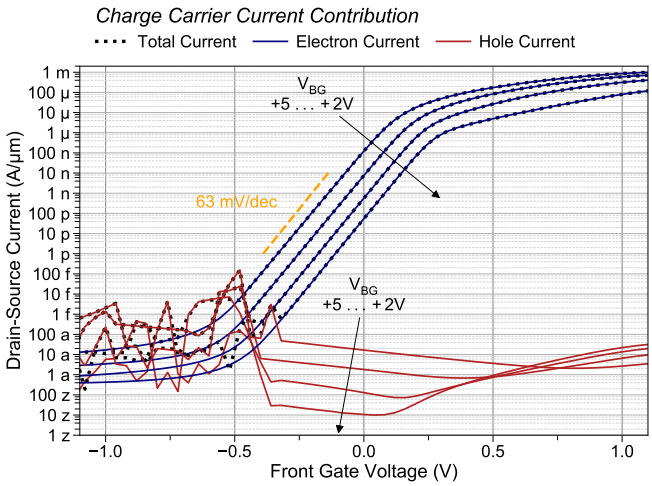
Further, as the carrier injection is exceptionally increased the FG output characteristic of the PMOS does not exhibit the typical supra-linear distortion normally found for SBH of 0.1 eV (Fig. 54). As the boron pile-up of the reference device at the SB interface and its eSBH increasing effect is still included in the simulation, the NMOS displays a supra-linear distortion for $V_{DS} < 0.75$ V.

Compared to experimentally reported NiSi SIDS-based SBFET, either long-channel devices [56] or short-channel devices [131, 142–145], the DeFET simulation shows similar $I_{DS,on}$ levels[a] although the WKB tunneling approximation model in conjunction with SBL results in a considerable I_{DS} current overestimation given the BOX thickness of 30 nm. As stated before, the predicted ideal sub-V_{th} slope has to be considered with caution as the implemented drift-diffusion model underestimates SCE. Nevertheless, the results hint quite favorable device performance and should be considered for future experimental research. As stated before, 0.1 eV SBH can be realized with NiSi SIDS-based process technologies in conjunction with selective ion implantation. Therefore, a co-integration of RFET and hard-wired high performance DeFET devices in a single technology process flow for optimized reconfigurable CMOS logic circuits seems feasible.

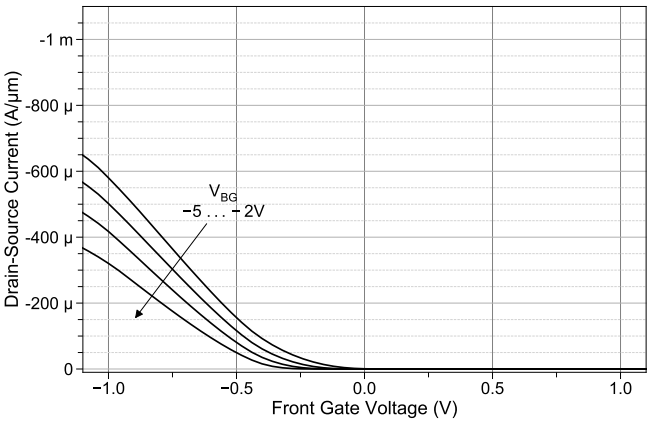
[a] Especially compared to Urban et al. [142, 144]



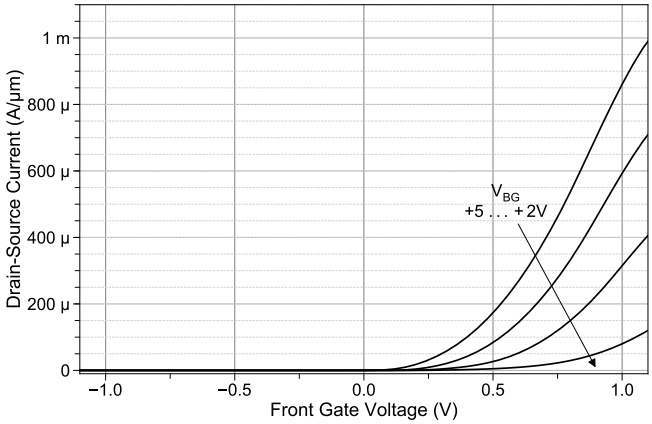
(a) Logarithmic plot, PMOS biasing $V_{\mathrm{DS}} = -1$ V



(b) Logarithmic plot, NMOS biasing $V_{\mathrm{DS}} = +1$ V

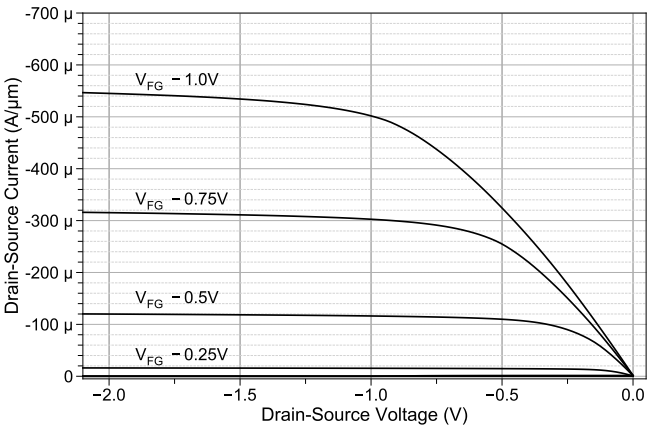


(c) PMOS biasing $V_{\mathrm{DS}} = -1$ V

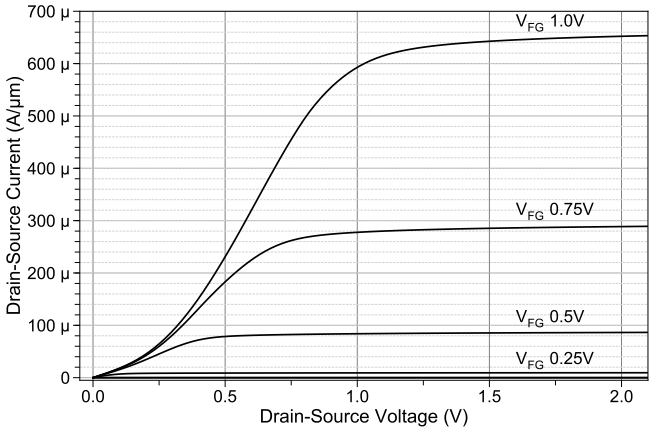


(d) NMOS biasing $V_{\mathrm{DS}} = +1$ V

Fig. 53: Effect of SBH 0.1 eV for electrons and holes, respectively, on FG input characteristics.



(a) PMOS biasing, $V_{\mathrm{BG}} = -4$ V, $V_{\mathrm{DS}} = -1$ V



(b) NMOS biasing, $V_{\mathrm{BG}} = +4$ V, $V_{\mathrm{DS}} = +1$ V

Fig. 54: Effect of 0.1 eV SBH for electrons and holes, respectively, on FG output characteristics.

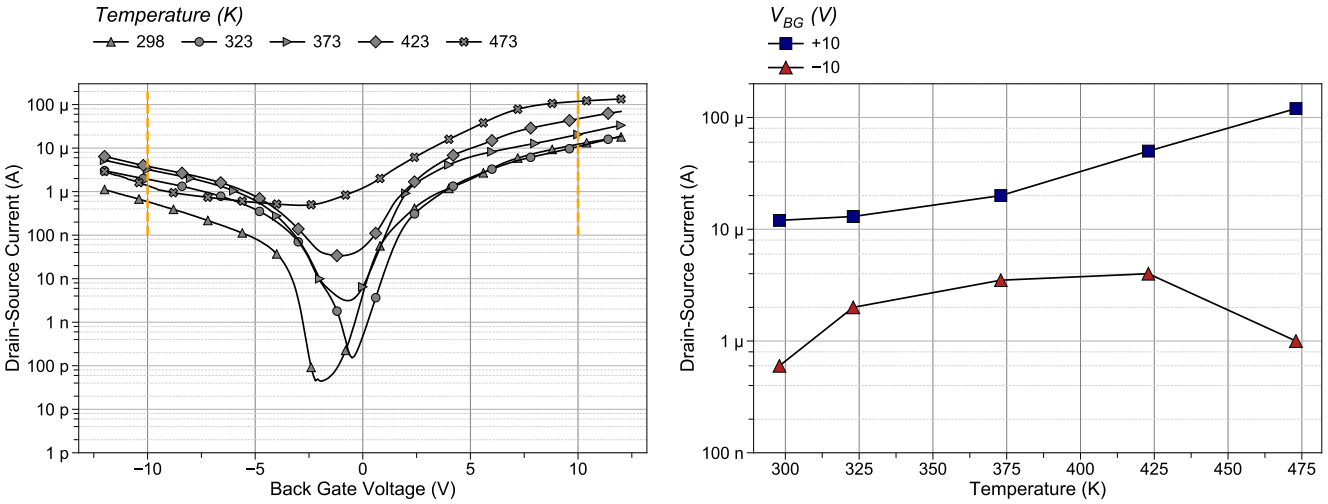
3.2.3 High Temperature Characteristics

In this section, the experimental results under high temperature (HT) conditions of long-channel POC devices are presented and compared followed by simulation results proposing the feasibility to implement hard-wired DeFET in conventional HT CMOS applications.

Due to the remarkably low off-state leakage currents ($I_{DS,off}$), the experimental DeFET devices exhibit exceptional characteristics under high operating temperatures. The reason for the exceptional HT performance lies in the SOI substrate, which eliminates the bulk leakage current as the main contributor to $I_{DS,off}$ leakage. Further, the introduction of SB contacts minimizes the leaking via the band-to-band tunneling effect in comparison to conventional steep S/D p-n junctions. In conjunction with the induced high potential barrier of the FG in the off-state, the $I_{DS,off}$ leakage is significantly reduced compared to conventional MOSFET designs (see Fig. 30).

In the following, experimental POC devices with aluminum and $WTiN_x$ FG electrodes of the 1st and 2nd generation with two different NiSi silicidation schemes are evaluated at substrate temperatures up to ~473 K (see 3.1).

As described in section 2.2.1, an increase in temperature raises the probability for charge carriers to overcome the SB by thermionic field emission (TFE) or thermionic emission (TE). Therefore, the carrier injection efficiency is exponentially enhanced and consequently the $I_{DS,on}$ current increases significantly. This mechanism is clearly illustrated by the BG input characteristic of a BG-only transistor for increased temperatures as depicted in Fig. 55.



(a) BG-only input characteristic, $V_{DS} = -1$ V

(b) $I_{DS,on}$ temperature dependency

Fig. 55: Input characteristics of a BG-only transistor at high temperatures, 2nd generation (RTA 60s). Dimensions: Width 100 µm, BGL 50 µm

The device exhibits a lower eSBH for electrons than for holes, typical for 2nd generation devices exposed only for 60 s to the RTA silicidation process. This results in a comparably reduced

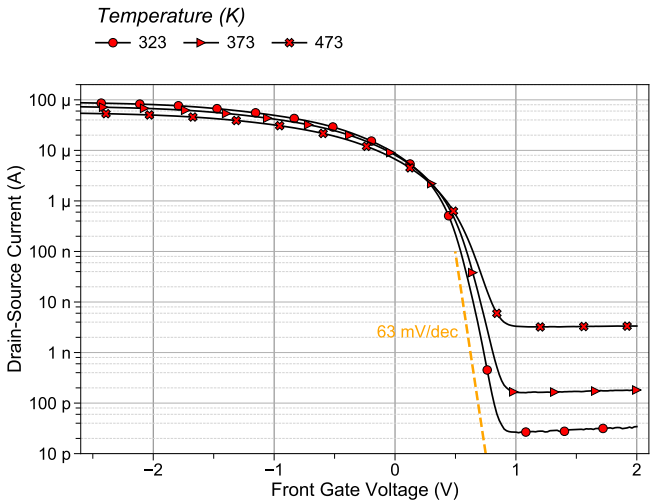
SIDS and boron pile-up formation as discussed previously. A rise of substrate temperature up to 473 K enhances $I_{DS,on}$ for NMOS operation (V_{BG} = +10 V) by up to an order of magnitude while for PMOS operation (V_{BG} = –10 V) the $I_{DS,on}$ increase saturates between 373 to 423 K and declines at 473 K (Fig. 55b). This decrease is attributed to the reduction of hole carrier mobility with increasing temperature while the increase of injection efficiency overcompensates this mobility decrease for electrons.

Fig. 56 depicts the FG high-temperature input characteristics of a 1st generation Al metal FG device with the SB fabricated by the horizontal furnace based silicidation process as described in 3.1. For NMOS operation (Fig. 56b,d) the $I_{DS,on}$ current increases from 11 µA at 323 K up to 78 µA at 473 K. As discussed before, the horizontal furnace silicidation process yielded SB devices with pronounced boron pile-up profiles due to SIDS and therefore an increased eSBH for electrons and reduced eSBH for holes. As the temperature is increased, the thermionic emission and thermionic field emission transport of electrons over and through the SB increases resulting in the increase of injection efficiency and consequently of $I_{DS,on}$ for the n-branch. On the other hand, for PMOS operation (Fig. 56a,c) the $I_{DS,on}$ current decreases with increasing temperature as the hole charge carrier mobility decreases and the SB injection efficiency is already maximized by the boron pile-up.

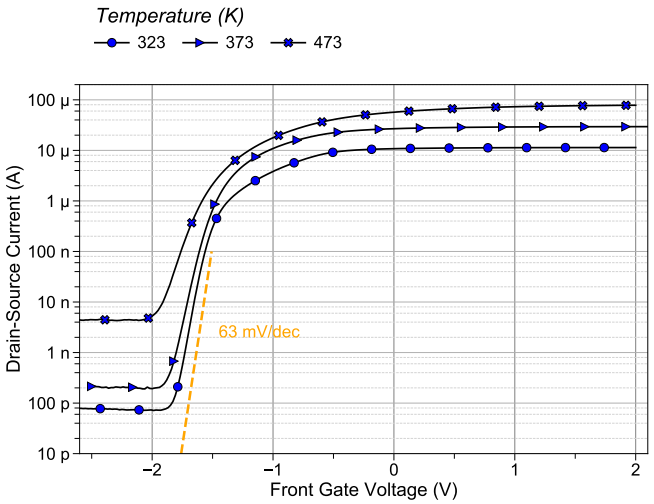
Notably, the electrostatic control of FG does not significantly deteriorate for increasing temperature as the sub-V_{th} slope does only increase moderately (Fig. 56a,b) and the FG output characteristic displays clear saturation behavior (Fig. 56e,f).

For both operation modes the $I_{DS,off}$ current increases by approximately 2 decades from 323 K to 473 K. It has to be noted, that the $I_{DS,off}$ leakage current at 323 K is initially already 2 decades higher compared to 2nd generation devices (e.g. Fig. 57). This is attributed to a larger Si-body thickness of 1st generation devices caused by a TMAH-based recess etch process deviation during the 1st generation device fabrication.

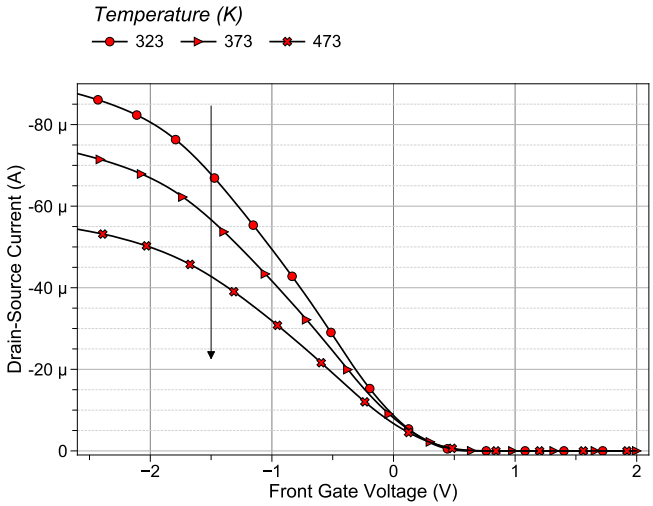
Especially for the NMOS operation, the typical supra-linear distortion of the FG output characteristic, which is associated with the drain-side SB, decreases and is completely compensated at 473 K as illustrated in Fig. 56 (compare with Fig. 34b, Fig. 54b).



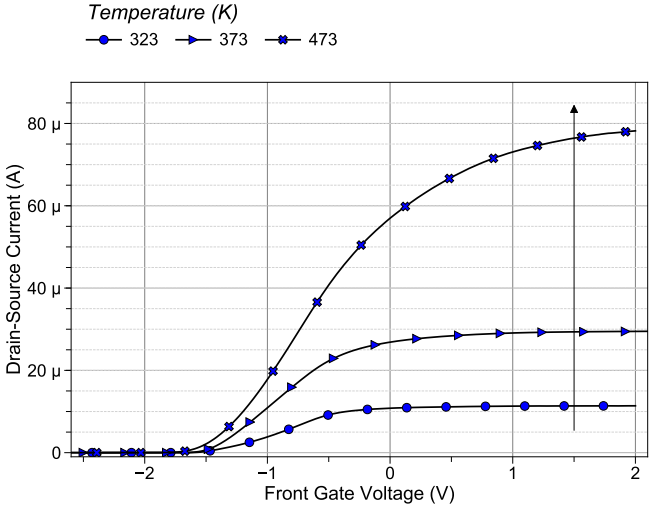
(a) Logarithmic plot, FG input characteristic
PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -20$V



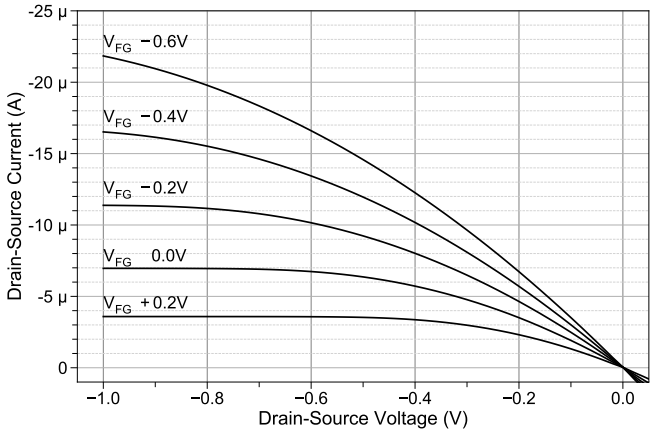
(b) Logarithmic plot, FG input characteristic
NMOS biasing $V_{DS} = -1$ V, $V_{BG} = +20$V



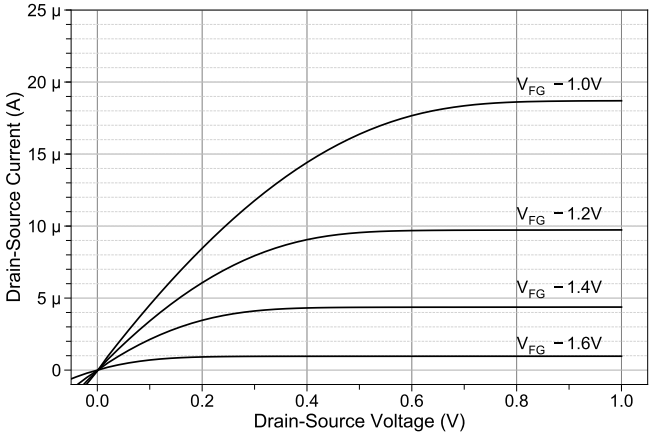
(c) Linear plot, FG input characteristic
PMOS biasing $V_{DS} = -1$ V, $V_{BG} = -20$V



(d) Linear plot, FG input characteristic
NMOS biasing $V_{DS} = +1$ V, $V_{BG} = +20$V



(e) FG Output characteristic at 473 K
PMOS biasing $V_{BG} = -20$V



(f) FG Output characteristic at 473 K
NMOS biasing $V_{BG} = +20$V

Fig. 56: Characteristics of an aluminum FG DeFET exposed to high-temperatures, 1st generation (furnace). Dimensions: Width 45 µm, BGL 34 µm, FGL 20 µm

The FG input characteristics under high temperature exposure of a 2nd generation DeFET are depicted in Fig. 57. The device exhibits a lower eSBH for electrons than for holes and is biased for $I_{DS,on}$ symmetry at room temperature with PMOS biasing of $V_{BG} = -18\,V$ and NMOS biasing of $V_{BG} = +12\,V$. For this biasing, both operation modes exhibit an increase of $I_{DS,on}$ offsetting and over compensating the decrease of carrier mobilities with increasing temperature (Fig. 57c,d). This demonstrates, that a careful selection of BG biasing or a temperature controlled BG biasing is able to minimize the negative temperature coefficient generally associated with MOSFET devices. In conjunction with the very temperature stable V_{th} and sub-V_{th}-slope, precise high temperature circuits are expected to be realizable. Nevertheless, device reliability has to be proven as well. As a matter of fact, $WTiN_x$ FG devices revealed reliability issues in form of FG_{Ox} dielectric breakdown at elevated temperatures further supporting the assumption of an oxide degrading effect of the reactive sputtering process.

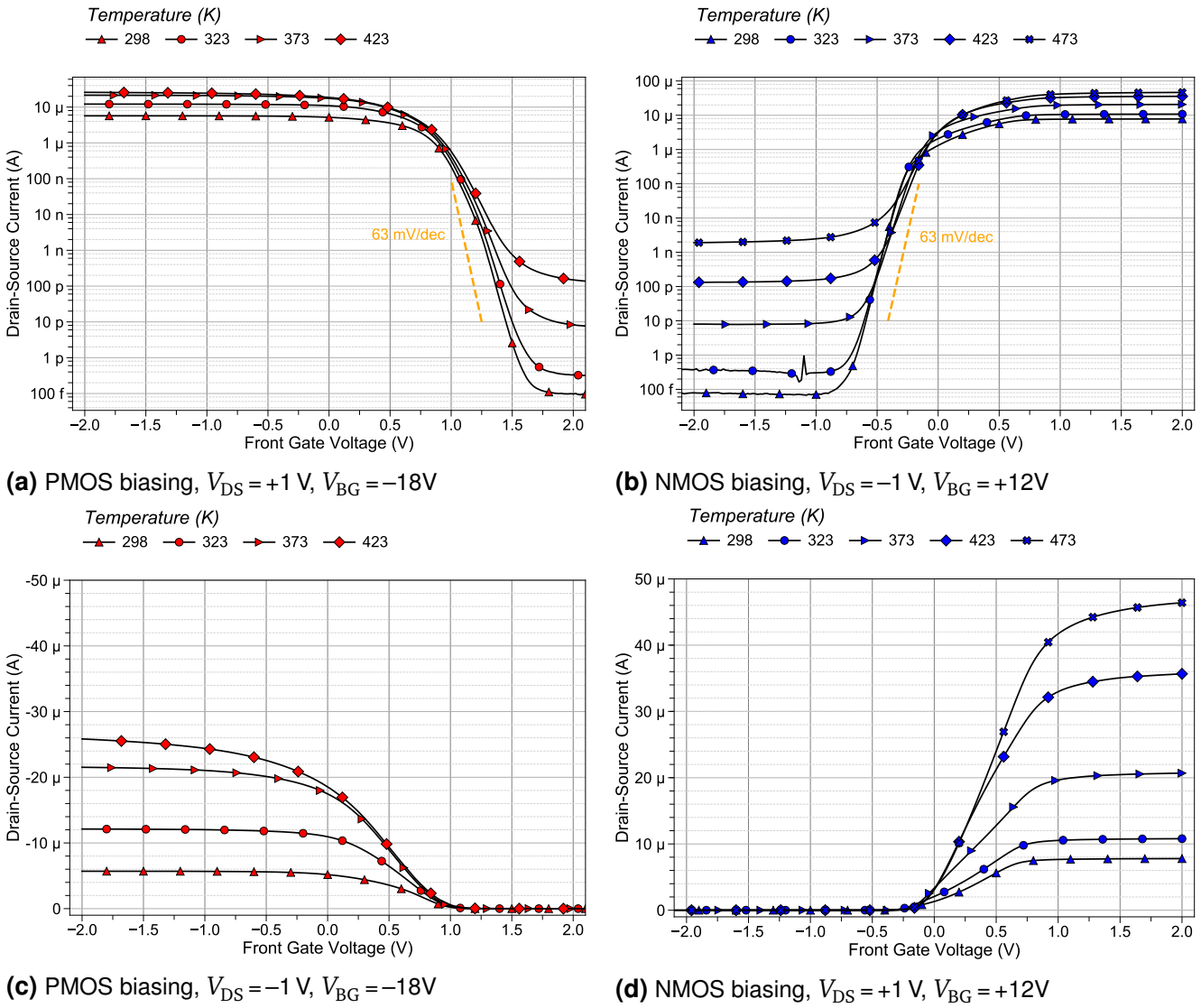
More over, compared to the 1st generation devices (Fig. 56), the $I_{DS,off}$ current is reduced by over 2 orders of magnitude at 323 K and one order of magnitude at 473 K for P- and NMOS operation (Fig. 57a,b). Again, this is linked to the fact, that the Si-body layer is considerable thinner compared to the 1st generation devices improving the electrostatic control of the FG on the channel.

Comparing the minimum $I_{DS,off}$ leakage current with reported long-channel silicon devices from the literature [146–148] provides an orientation for the high temperature performance in terms of $I_{DS,off}$ leakage suppression of the DeFET concept as depicted in Fig. 58a [95]. The referenced devices feature similar micrometer gate lengths but differ in other leakage performance affecting parameters as gate oxide thickness, doping and device architecture, i.e. FinFET, NW and planar devices. Therefore, the comparison to these devices should be considered as a first estimation. As experimentally demonstrated, the DeFET offers over one order of magnitude less leakage current compared to the next best NW JLFET design [147]. Directly compared to the predecessor NW RFET of F. Wessely, the 1st generation DeFET exhibits a similar behavior [16]. But, as the Si-body layer has been successfully reduced for the 2nd generation DeFET devices, an improvement of 3 decades from 1 pA/µm to 1 fA/µm at room temperature and >1 decade at elevated temperatures is achieved. Further, the $I_{DS,on}$ current follows an opposite trend and increases for increasing temperatures as the SB injection efficiency raises for the moderately chosen BG potential of +12 V in contrast to the $V_{BG} = +20\,V$ of the NW RFET (Fig. 58b).

As an additional reference, state-of-the-art industrial HT MOSFET devices of XREL Semiconductor are electrically characterized on bare dice level. The XTR2N0807NA20[a] features an estimated gate width of 8x 1200 µm (~9600 µm) as derived from Fig. 59a [149]. The device offers an impressive on/off current ratio of 10 decades compared to ~8 decades of the experi-

[a] Devices are pre-series production samples and final series performance may vary.

mental DeFET devices. As discussed previously, this ratio is directly linked to the inefficient SB carrier injection. Substituting the mid-gap SB against 0.1 eV eSBH contacts potentially results in theoretical 15 decades and substantial $I_{\mathrm{DS,Drive}}$ current (see Fig. 53). In terms of $I_{\mathrm{DS,off}}$ leakage current both devices demonstrated almost identical exceptional performance (Fig. 58a).



(a) PMOS biasing, $V_{\mathrm{DS}} = +1$ V, $V_{\mathrm{BG}} = -18$V

(b) NMOS biasing, $V_{\mathrm{DS}} = -1$ V, $V_{\mathrm{BG}} = +12$V

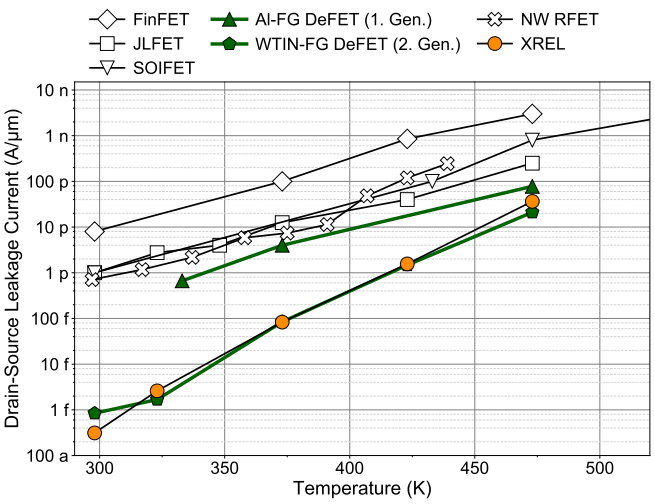
(c) PMOS biasing, $V_{\mathrm{DS}} = -1$ V, $V_{\mathrm{BG}} = -18$V

(d) NMOS biasing, $V_{\mathrm{DS}} = +1$ V, $V_{\mathrm{BG}} = +12$V

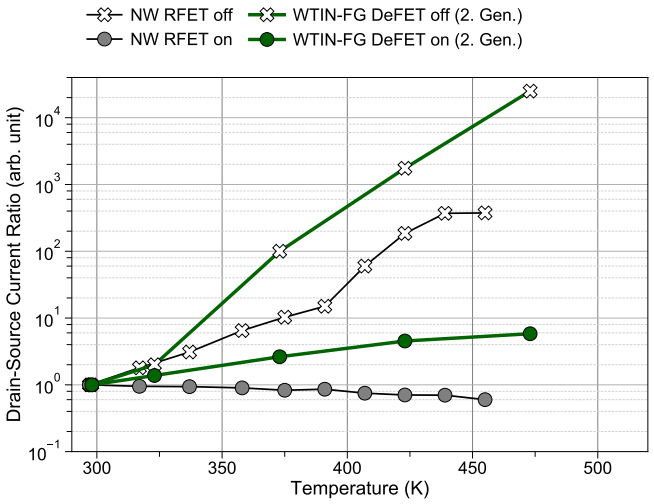
Fig. 57: FG input characteristics for a $WTiN_x$ FG device (NiSi RTA, 60s) exposed to high-temperatures. Dimensions: Width 100 µm, BGL 90 µm FGL 5 µm

In order to gather predictive results regarding the HT performance of the DeFET beyond 473 K, TCAD simulations based on a less scaled[a] dual-gate DeFET device are conducted. Extending the DD simulations into high temperature regions normally requires an extensive temperature calibration of the simulation parameters. As this is not implemented at this point, results have to be regarded as trends with a considerable uncertainty although HD simulations do not differ significantly from the here presented DD based simulations. As transistor reconfigura-

[a] FGL 180 nm, underlap 40 nm, BGL 260 nm, BOX 30 nm, Si-body 7 nm, $\mathrm{FG_{Ox}}$ 1 nm



(a) $I_{\mathrm{DS,off}}$ leakage current comparison derived from Fig. 57a,b and Fig. 56a,b. Referenced long-channel devices: FinFET by Akarvardar et al. [148], JLFET by Lee et al. [147], SOIFET by Flandre et al. [146] and NW RFET by Wessely et al. [16, p.110].



(b) Comparison of RFET $I_{\mathrm{DS,off}}$ and $I_{\mathrm{DS,on}}$ currents normalized to 323 K derived from Fig. 57. NW RFET characteristics taken from F. Wessely et al. [16, p.107] for conventional V_{DS} biasing.

Fig. 58: Summarized temperature dependencies.

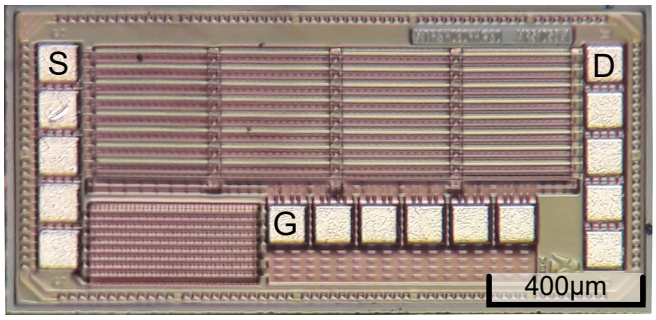
bility under HT conditions is not of primary interest, the optimizations presented earlier for conventional CMOS applications are implemented and discussed.

Fig. 60a,b illustrates the FG input characteristics for elevated temperatures of a dual-gate DeFET with mid-gap SB contacts. As stated before, the high $I_{\mathrm{DS,CMOS-Off}}$ and the $\mathrm{on/off_{CMOS}}$ ratio of only 2 decades are not suited for CMOS circuit design.

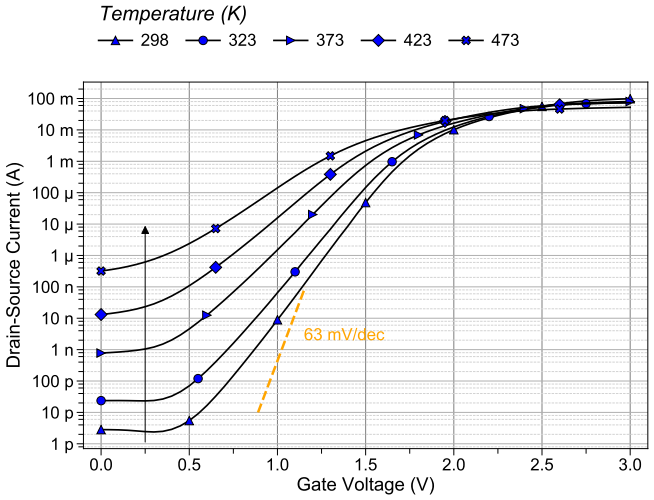
By applying the previously presented FG work function (FGWF) engineering, the high $I_{\mathrm{DS,CMOS-Off}}$ is mitigated and results in theoretically only <10 nA/µm leakage current and still over 3 decades of $\mathrm{on/off_{CMOS}}$ current ratio even at 550 K (Fig. 60c,d).

Combining the FG work function engineering with 0.1 eV eSBH for holes and electrons, respectively, leads to extraordinary theoretical FG input characteristics as depicted in Fig. 61. Besides the high $I_{\mathrm{DS,on}}$, the $I_{\mathrm{DS,off}}$ branch is further reduced below 10 pA/µm at 500 K, as ambipolar injection at the drain-side is efficiently suppressed. Note, as SB injection efficiency is already maximized, the $I_{\mathrm{DS,on}}$ current decreases due to reduced carrier mobilities for rising temperatures.

By combining all the previously presented theoretical improvements, the resulting DeFET device with remarkable HT characteristics for conventional HT CMOS applications is regarded as a promising research candidate. In the next section, as part of an outlook, another promising candidate is discussed.

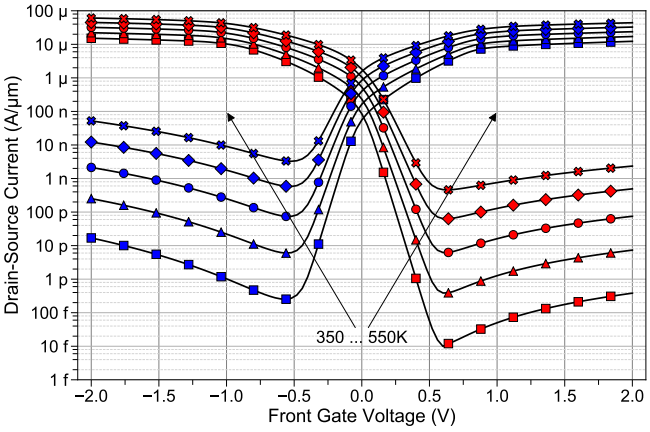


(a) Optical micrograph of bare dice

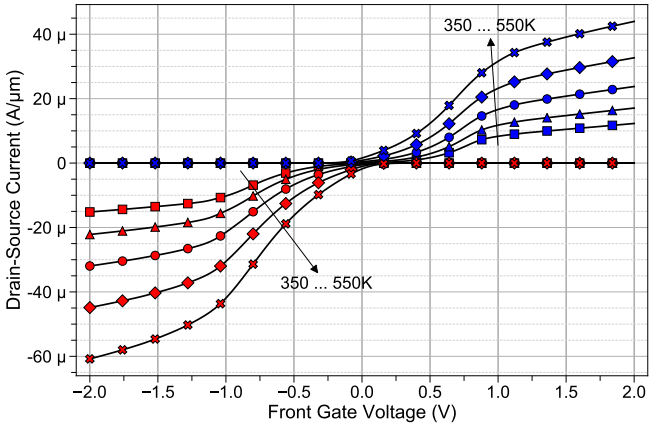


(b) Logarithmic plot, NMOS input characteristics, $V_{DS} = -1$ V

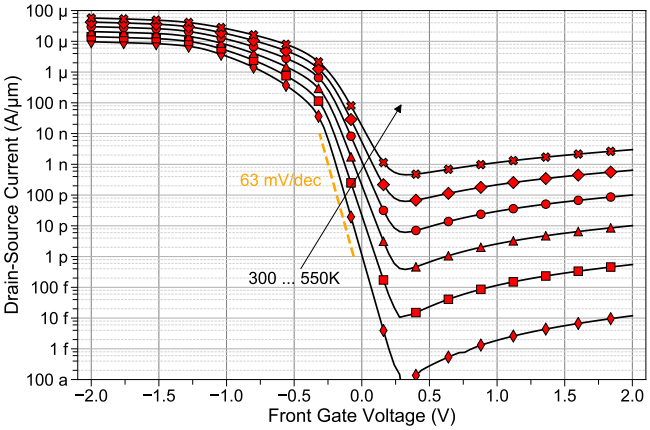
Fig. 59: Optical micrograph and input characteristics of a HT industrial grade XREL XTR2N0807NA20 n-type MOSFET (pre-series production) exposed to high temperatures.



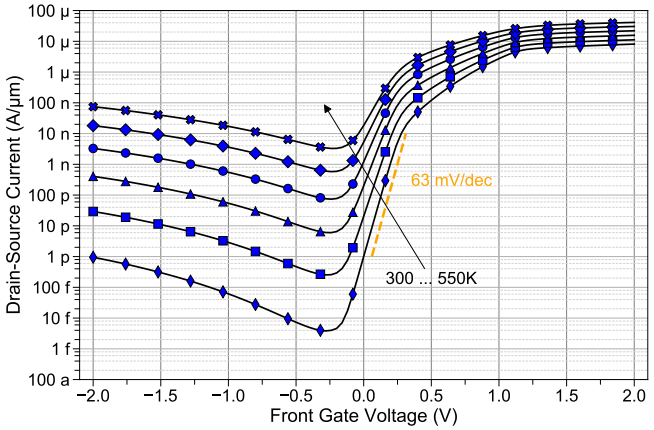
(a) Logarithmic plot, $V_{DS} = +/-1$ V, $V_{BG} = +/-5$ V



(b) linear plot, $V_{DS} = +/-1$ V, $V_{BG} = +/-5$ V

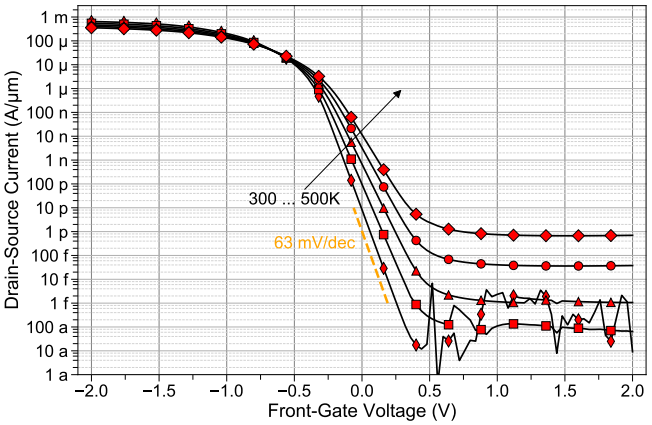


(c) Logarithmic plot, FG input characteristics FGWF 4.38eV, $V_{DS} = -1$ V, $V_{BG} = -5$ V

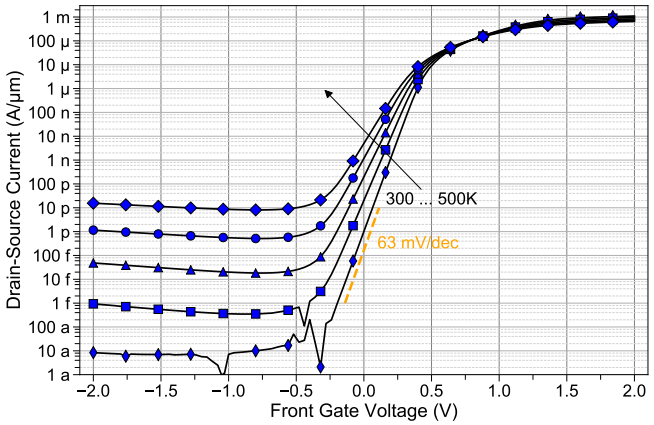


(d) Logarithmic plot, FG input characteristics FGWF 4.98eV, $V_{DS} = +1$ V, $V_{BG} = +5$ V

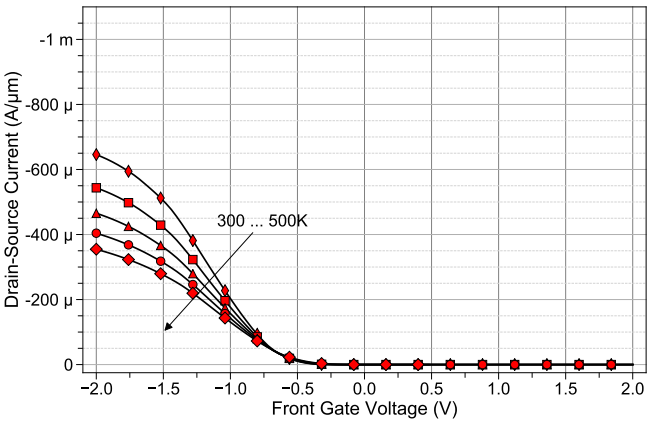
Fig. 60: Effect of temperature on dual-gate DeFET FG input characteristics (FGL 180nm) without and with optimized FGWF.



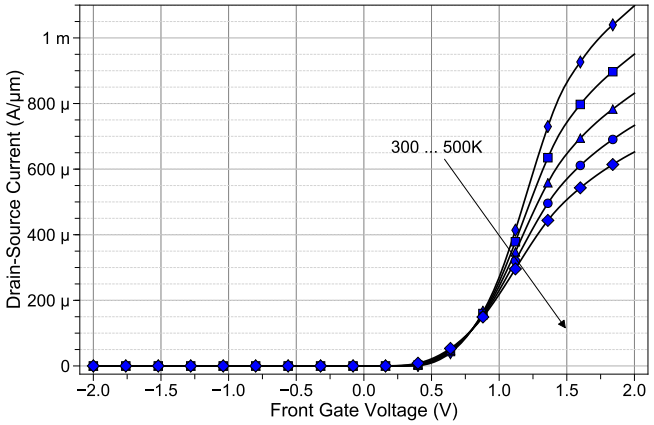
(a) Logarithmic plot, PMOS FG characteristics
FGWF 4.38eV, eSBH 0.1 eV, $V_{DS} = -1$ V, $V_{BG} = -5$ V



(b) Logarithmic plot, NMOS FG input characteristics
FGWF 4.98eV, eSBH 0.1 eV, $V_{DS} = +$ V, $V_{BG} = +5$ V



(c) linear plot, PMOS FG input characteristics
FGWF 4.38eV, eSBH 0.1 eV, $V_{DS} = -1$ V, $V_{BG} = -5$ V



(d) linear plot, NMOS FG input characteristics
FGWF 4.98eV, eSBH 0.1 eV, $V_{DS} = +1$ V, $V_{BG} = +5$ V

Fig. 61: Effect of temperature on FGL 180 nm FG input characteristics for low eSBH and optimized FGWF.

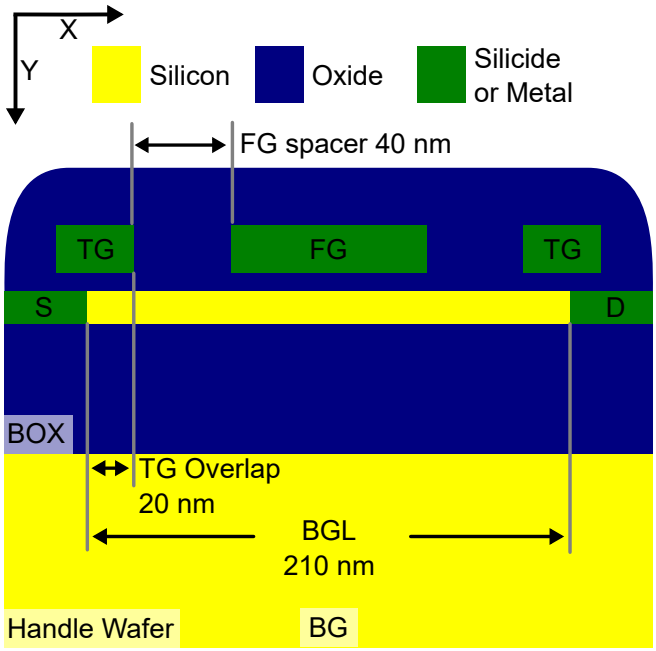
3.2.4 High Performance 2.5-Gate DeFET Device

In this section, as part of an outlook for the reconfigurable DeFET approach, an advanced planar DeFET structure is proposed and briefly evaluated by means of TCAD device simulations [97, 105]. The device is able to mitigate the low $I_{\mathrm{DS,Drive}}$ current of the mid-gap SB contacts as well as the low threshold voltage, which results in a high $I_{\mathrm{DS,CMOS-Off}}$ current of the dual-gate reconfigurable DeFET in conjunction with the SB resistance limited sub-V_{th} slope. The proposed planar DeFET design exhibits similarities to the stacked silicon nanowire based approach presented by De Marchi et al. [89, 90] but features a distinct additional BG electrode for V_{th} shifting that is generally not efficiently applicable to nanowire based approaches and a unique feature of planar FDSOI and, less effective, of bulk MOSFET devices [15, 88].

In the 2.5-gate DeFET structure, two additional top gate (TG) electrodes are implemented, clamping the SB of S/D electrostatically between the BG and TG (Fig. 62a). For the 2.5-gate variant, the BG and TG are biased identically, reducing layout and routing complexity compared to the separately biasable triple-gate approach. For the triple-gate DeFET, the gate potentials can be selected independently, allowing independent adjustments of V_{th} and $I_{\mathrm{DS,on}}$ as well as enabling the implementation of two logic inputs per DeFET device. But, by this approach, the circuit layout complexity is significantly increased [92, 150]. On the other hand, biasing the TG by the source potential could compensate on the layout complexity as discussed by Moura et al. [151]. In the following discussion, the focus is laid on the 2.5-gate approach based on design parameters summarized in Fig. 62b.

In contrast to previous device simulations, the following subset of device simulations feature the physically founded Schrödinger instead of the WKB SB tunneling model. This is based on the fact, that the increased electrostatic control on the SB results in implausible high $I_{\mathrm{DS,on}}$ currents due to the severely violated wide barrier assumption of the WKB approach resulting in a considerable overestimation of injection efficiency. Following the argumentation of R. Vega, the light hole sub-band is considered to dominate the hole carrier transport over the SB for the Schrödinger model. Hence, effective tunneling masses for electrons (m^*_{tn}) and holes (m^*_{tp}) are set to 0.19 m_0 and 0.16 m_0 , respectively [122, pp.13]. Similar to the previous simulations, a SIDS boron pile-up with a peak concentration of 5e18 cm^{-3} is introduced to the body layer at the SB interfaces in order to realize symmetric p- and n-branch characteristics.

The simulated BG & TG input characteristics, as depicted in Fig. 63a, illustrate the improved electrostatic control on the SB contacts in comparison to the BG-only input characteristics, which are simulated with identical parameters and model framework. The $I_{\mathrm{DS,on}}$ currents increase by ~3 orders of magnitude from 60 nA/µm to 200 µA/µm for PMOS ($V_{\mathrm{BG}} = -3$ V) and 40 nA/µm to 300 µA/µm for NMOS operation ($V_{\mathrm{BG}} = +3$ V) (Fig. 36a). These increases result



(a) Schematic tripple- or 2.5-Gate DeFET structure

Parameter	Unit	Value
FG work function	eV	4.68
FG length	nm	90
FG spacer	nm	40
FG_{Ox} thickness	nm	2
TG length	nm	40
TG overlap	nm	20
BG Length	nm	210
Body layer thickness	nm	7
BOX thickness	nm	30
Electron SB height (ϕ_{Bn})	eV	0.63
m^*_{tn} / m^*_{tp}	m_0	0.19 / 0.16

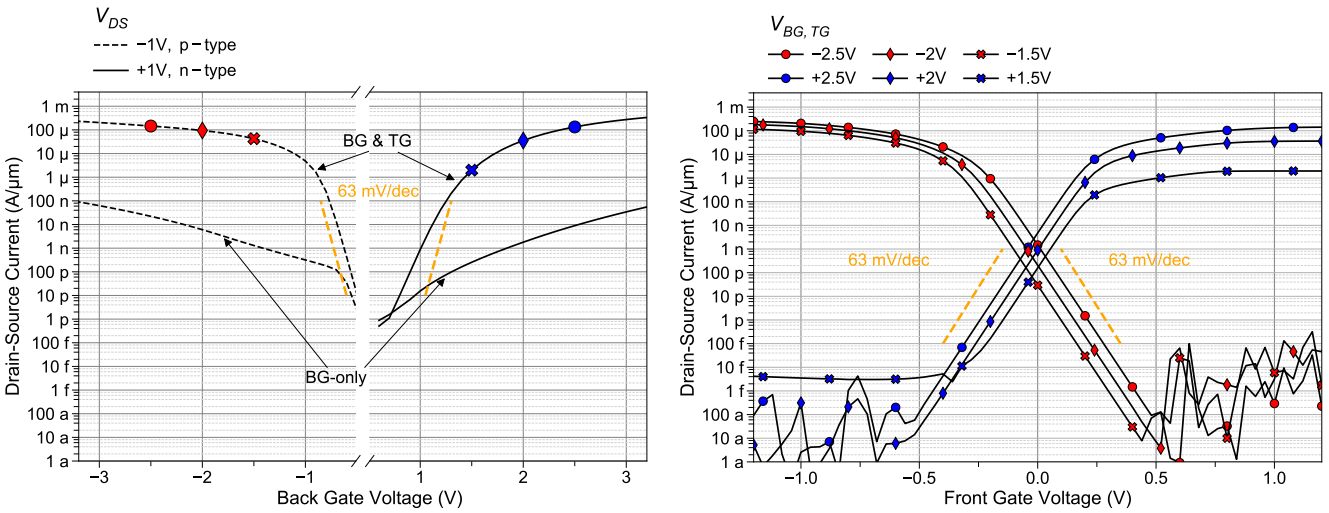
(b) 2.5G DeFET simulation parameters

Fig. 62: Schematic tripple- or 2.5-Gate DeFET structure and simulation parameters.

from significantly decreased tunneling distances at the source SB, as illustrated by the band diagrams for PMOS (Fig. 64a) and NMOS operation (Fig. 64b). Noteworthy, the sub-V_{th} slope is also significantly decreased close to the ideal 63 mV/dec limit for the p-branch by the reduced effective SB resistance (compare Fig. 36a).

As less BG potential is necessary to electrostatically modulate the SB to achieve reasonable $I_{DS,on}$ magnitudes, the FG_{Ox} thickness requirements are reduced as well (see Fig. 39b). Therefore, the following results are derived from simulations with 2 instead of 1 nm EOT FG_{Ox} thickness, possibly reducing the technological fabrication complexity as only mid-κ instead of high-κ dielectrics would be required. Further, the reduction of V_{BG} allows an increase of V_{th} and, given the ideal sub-V_{th} slope, a decrease of $I_{DS,CMOS-Off}$ below $< 4\,nA/\mu m$ as illustrated by the FG input characteristics in Fig. 63b (compare Fig. 36b). More over, the CMOS on-to-off current ratios are increased from 3 to 5 decades theoretically enabling reconfigurable CMOS circuit designs with sufficient noise immunity and low static power consumption. Again, the V_{th} shiftability of $125\,mV/V_{BG}$ is able to reduce $I_{DS,CMOS-Off}$ by over one order of magnitude facilitating dynamic switching between low-power and high-performance circuit states as it is the case in modern FDSOI CMOS technologies [15].

In comparison to the simulation results of dual-gate DeFET devices with SB heights of 0.1 eV for conventional CMOS applications in subchapter 3.2.2, the reconfigurable mid-gap SB 2.5-gate DeFET offers slightly less $I_{DS,on}$ current (compare Fig. 52, Fig. 53 with Fig. 63). But, this result is less compelling as the WKB model implemented for the dual-gate 0.1 eV SBH simulations tends to overestimate the $I_{DS,on}$ current. Therefore, an exemplary comparison based on



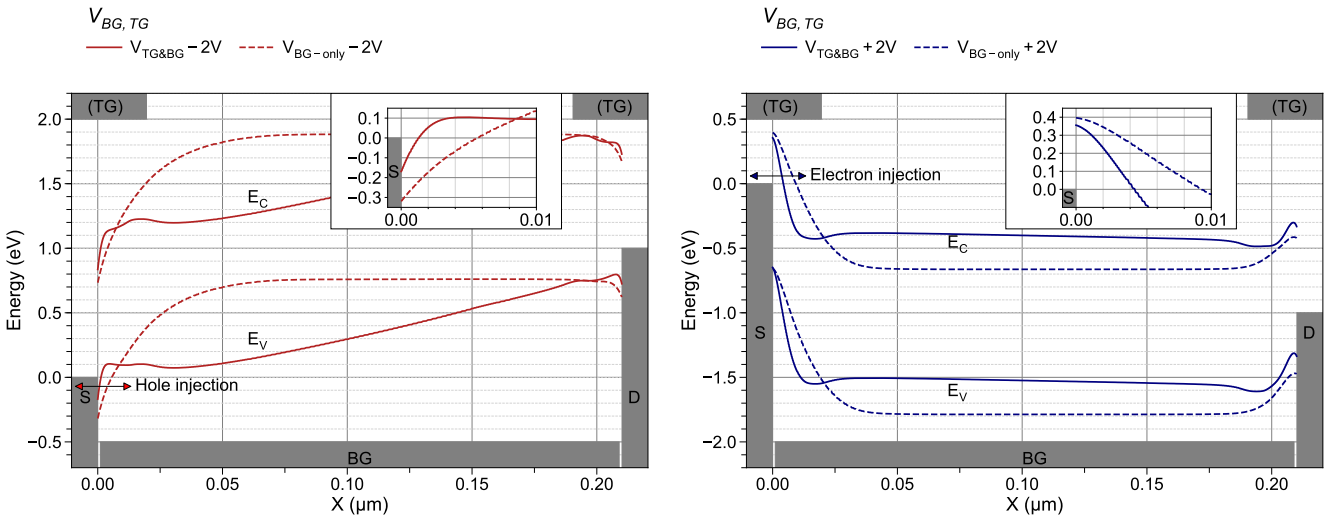
(a) Logarithmic plot, BG & TG input characteristics

(b) Logarithmic plot, FG input characteristics, $V_{DS} = \pm 1$ V

Fig. 63: Simulated BG-only, combined BG & TG and FG input characteristics of a 2.5-gate DeFET device.

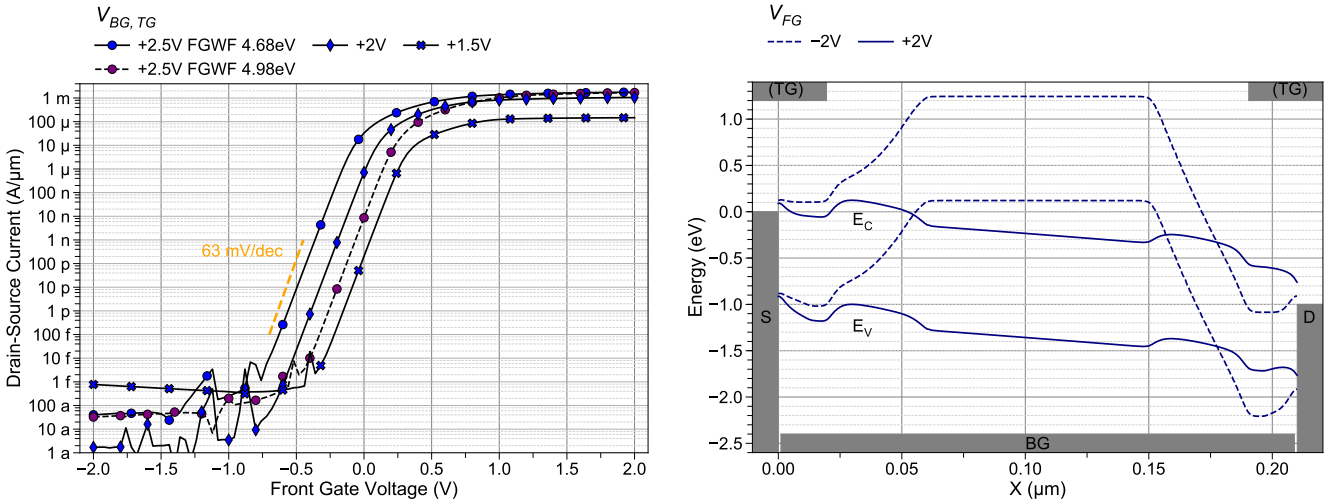
the Schrödinger model for optimized 2.5-gate NMOS operation with 0.1 eV SBH is depicted in Fig. 65. Although the Schrödinger model is more conservative, the $I_{DS,on}$ currents are on par with the WKB-based dual-gate DeFET approach (compare Fig. 53 with Fig. 65a). Also, as previously described (see Fig. 44), FGWF engineering is able to reduce the $I_{DS,CMOS-Off}$ by over 3 decades to 10 nA/µm for $V_{BG} = +2.5$ V (Fig. 65a, compare blue and green circle). Further, the TG electrode effectively shields the SB from the stray electric field of the FG electrode, as the nearly flat conduction energy band at the source side for $V_{FG} = -2$ V (off-biasing) indicates in Fig. 65b. This results in a reduction of the required spacer distance without leading to an ambipolar leakage current increase, as observed for the dual-gate DeFET (see Fig. 43).

Eventually, the simulatively proposed 2.5-gate DeFET has to be verified experimentally to finally conclude on the device performance. A possible fabrication approach could be based on a conventional spacer self-aligned gate-first process by introducing a second and third spacer formation step in order to obtain a top side gate stack with the FG capped by the TG electrode and the TG dielectric. A TCAD based process development as well as refined device simulations are part of the DFG funded PARFAIT cooperation project [152].



(a) PMOS biasing, $V_{DS} = -1$ V **(b)** NMOS biasing, $V_{DS} = +1$ V

Fig. 64: Simulated 2.5-gate device band diagrams for TG & BG and BG-only configuration parallel to the body-to-BOX interface at 3 nm inside the Si-body layer at 323 K (compare Fig. 63a). Insets illustrate the source contact in detail.



(a) NMOS, $V_{DS} = +1$ V, SBH 0.1 eV **(b)** NMOS, $V_{BG} = +2.5$ V, SBH 0.1 eV, FGWF 4.98 eV

Fig. 65: Simulated 2.5-gate device FG input characteristic and corresponding band diagrams for V_{FG} ±2 V and 0.1 eV SBH. Band diagram cut line parallel to the body-to-FG_{Ox} interface at 1 nm inside the Si-body layer at 323 K.

4 Conclusion and Outlook

4.1 Conclusion

This work contributes to the intensifying research on the feasibility of extending Moore's law by exploiting novel characteristics of polarity controllable or reconfigurable MOSFET (RFET). Generally, RFET devices are able to switch between n- and p-type conduction during circuit operation via an ordinary electrical signal. Therefore, RFET enable increased complex systems while decreasing the costs per basic logic function, based on their higher logic expressiveness. Unlike the majority of research efforts in this field, which are concentrating on extending end-of-roadmap *silicon nanowire* and *gate-all-around* RFET structures, this work focuses on leveraging the economically matured and established *planar* FDSOI technology.

The scope of the work presented here includes the successful transfer of a predecessor silicon nanowire RFET technology into a *planar* RFET device termed DeFET. Additionally, this technology is evaluated and optimized by means of experiments and TCAD simulations for reconfigurable, as well as conventional CMOS device operation. In direct comparison to the predecessor technology, the experimentally realized DeFET performance is further improved regarding sub-V_{th} slope, $I_{\mathrm{DS,off}}$ and high temperature (HT) characteristics. Also, the process complexity is significantly reduced as standard UV, instead of electron beam lithography, is sufficient for planar fabrication.

Based on a flexible non-self-aligned gate fabrication process, various proof-of-concept designs and two functional DeFET device generations have been realized. The influence of different front gate electrode materials, i.e. nickel, aluminum and reactively sputtered $\mathrm{WTiN_x}$ in single- and as dual-metal front gate designs, is successfully experimentally demonstrated. Notably, $\mathrm{WTiN_x}$ is identified as a possible mid-gap work function gate material suited for symmetric RFET device design. In the context of n- and p-branch symmetry, the effective Schottky barrier height adjustment process via SIDS is experimentally verified to be capable of delivering highly balanced SB properties, which is essential for adequate RFET CMOS circuit design.

Based on the simulative design space exploration, a sufficiently thin ($\ll 7\,\mathrm{nm}$) body layer is identified as the most critical feature of the planar dual-gate DeFET device design in order to realize a sufficient $\mathrm{on/off_{CMOS}}$ current ratio and low $I_{\mathrm{DS,CMOS-Off}}$ static leakage current levels for reconfigurable circuits. Also, the introduction of a dual-metal front gate electrode theoretically results in a proper CMOS device performance but unfortunately the experimental results can only partly confirm this prediction due to complex process variations of the $\mathrm{WTiN_x}$ reactive sputter deposition process. Based on experimental results of the NiSi SB formation in conjunction with SIDS, a possible route for a co-integration of hard-wired low SBH high-performance DeFET, with increased $I_{\mathrm{DS,on}}$ for conventional CMOS circuits building blocks side by side with reconfigurable DeFET blocks in one fabrication process flow, is simulatively proposed.

In comparison with the predecessor NW RFET devices, the HT performance of the DeFET has been significantly improved. Especially the $I_{DS,off}$ leakage current under HT conditions is experimentally demonstrated to be on par with industrial grade HT MOSFET devices. Moreover, the simulative combination of low SBH and suitable FGWF for hard-wired P- and NMOS DeFET results in impressive characteristics for HT CMOS applications.

Last but not least, the 2.5-gate DeFET concept offers predictively superior RFET performance compared to the dual-gate DeFET design as $I_{DS,CMOS-Off}$, sub-V_{th} slope and $I_{DS,Drive}$ are almost on par with conventional FDSOI MOSFET technologies. However, this prediction has to be considered with caution as no experimental verification is available, today.

4.2 Outlook

The results presented in this thesis suggest reasonable prospects for a possible extension of Moore's law by planar FDSOI-based reconfigurable DeFET devices. Based on these prospects, the cooperation project *PARFAIT: Power-aware AmbipolaR Fpga ArchITecture*, currently executed by the ITIV (KIT) together with the IES (TUD) and ISTN (TUD), has been granted and completely funded for three years by the DFG (Fig. 66).

The PARFAIT project builds upon the initial development of a predictive technology model (PTM) via physically motivated TCAD simulations and the extension of the block-based into process-based TCAD simulations. The PTM is the virtual equivalent to a hardware derived process design kit (PDK), typically provided by semiconductor foundries for circuit design and layout. In this context, further device optimizations including triple-gate DeFET arrangements are considered. A noteworthy advantage of the tripple-gate DeFET is the intrinsic XOR functionality on transistor level, which is frequently used by en/decryption, checksum calculation and other arithmetic operations. Based on the derived PTM, the benefits of transistor level reconfigurability for circuit design and system architecture of, but not limited to, FPGA are evaluated with a focus on a reduction of chip area and power consumption. As the DeFET technology features a wide threshold shiftability, a threshold adaption scheme for dynamic circuit delay compensation and leakage current optimization, both at the design- and run-time, is evaluated. This theoretically enables FPGA designs to cope with delay variation caused by temperature changes and on-chip-variation. Also, the reconfigurability is considered for improving the performance and reduce the area overhead of the FPGA interconnect network. Last but not least, as the electrostatic instead of chemical doping concept in conjunction with SB contacts prevents the carrier freeze-out effect at cryogenic temperatures. Therefore, cryogenic and high operating temperature for digital applications in harsh environments are studied as well within this project.

Besides the simulative approach of the PARFAIT project, further hardware based studies of the DeFET technology in the context of sensing, harsh environment and high frequency operation are interesting future research topics. Especially the shiftable steep sub-threshold operation region and freely selectable charge carriers for sensing applications and the low parasitic capacitances of the front gate and SB contacts for high frequency operation suggest promising insights.

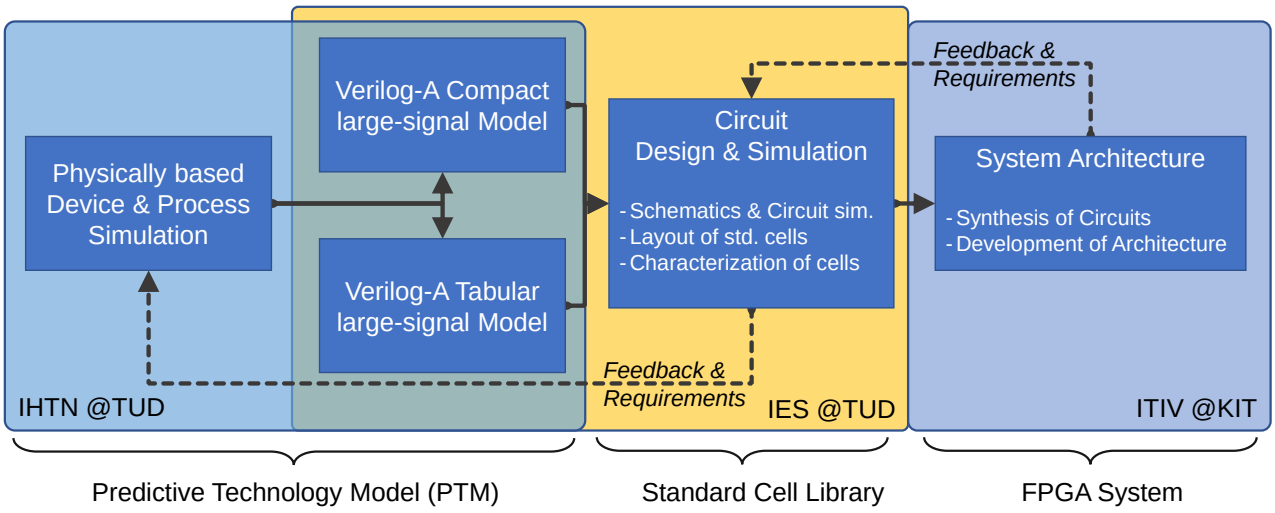


Fig. 66: Project flow of the DFG funded PARFAIT project.

Directories

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List of Abbreviations

BG	Back-gate
BGL	Back-gate length
BOX	Buried (silicon) oxide
CG	Control gate
CMOS	Complementary metal-oxide-semiconductor
$CoSi_2$	Cobald di-silicide
CVD	Chemical vapor deposition
DC	Direct Current
DD	Drift-diffusion carrier transport model
DeFET	Dehancement mode field-effect transistor
DFG	Deutsche Forschungsgemeinschaft
DUT	Device Under Test
ED	Electrostatic doping
EOT	Equivalent (Silicon) Oxide Thickness
ERD	Emerging research devices
$ErSi_2$	Erbium di-silicide
eSBH	effective Schottky barrier height
FD	Fully depleted
FDSOI	Fully depleted SOI
FE	Field emission
FET	Field-effect transistor
FG	Front gate
FGL	Front gate length

FG_{Ox}	Front gate oxide
FGWF	Front gate work function
FinFET	Fin field-effect transistor
FOM	Figure of merit
FPGA	Field programmable gate array
HD	Hydrodynamic carrier transport model
HF	Hydrofluoric acid
HT	High temperature
IES	Integrated Electronic Systems Lab
ISTN	Institute for Semiconductor Technology and Nanoelectronics
ITIV	Institut für Technik der Informationsverarbeitung (institute for techniques of information processing)
ITRS	International Technology Roadmap for Semiconductors
JLFET	Junctionless field-effect transistor
KIT	Karlsruhe Institute of Technology
MISFET	Metal-insulator-semiconductor FET (or MOSFET)
MOS	Metal-oxide-semiconductor
MOSCAP	Metal-oxide-semiconductor capacitor
MOSFET	Metal-oxide-semiconductor FET (or MISFET)
$MoTe_2$	Molybdenum di-telluride
Ni_2Si	Dinickel silicide
NiSi	Nickel silicide
$NiSi_2$	Nickel disilicide
Ni_xSi_y	Nickel silicide alloy
NMOS	n-type or electron channel MOSFET
NW	Nanowire
on/off_{CMOS}	CMOS On-to-off current ratio ($I_{DS,Drive}/I_{DS,CMOS-Off}$)

PARFAIT	Power-aware AmbipolaR Fpga ArchITecture
PD	Partly depleted
PDK	Process design kit
PG	Program gate or polarity gate
PMOS	p-type or hole channel MOSFET
POC	Proof of Concept
PTM	Predictive technology model
PtSi	Platinum silicide
PVD	Physical vapor deposition
RFET	Reconfigurable FET
RTA	Rapid thermal annealing
S/D	Source/drain
SB	Schottky barrier
SBFET	Schottky barrier field-effect transistor
SBH	Schottky barrier height
SBL	Schottky barrier lowering
SCE	Short channel effects
SIDS	Silicidation-induced dopant segregation
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
TCAD	Technology computer aided design
TE	Thermionic emission
TFE	Thermionic-field emission
TG	Top-gate
$TiSi_2$	Titan disilicide
TMAH	Tetramethylammonium hydroxide
TUD	Technical University Darmstadt

ULSI	Ultra large scale integration
UV	Ultraviolet
WKB	Wentzel-Kramers-Brillouin
WSe_2	Tungsten diselenide
WTi	Tungsten-titanium
$WTiN_x$	Tungsten-titanium-nitride
$YbSi_2$	Ytterbium disilicide

List of Symbols

χ_S	Electron Affinity of Semiconductor
$\Delta\phi$	Barrier Lowering in thermal equilibrium
$\Delta\phi_F$	Barrier Lowering under forward bias
$\Delta\phi_R$	Barrier Lowering under reverse bias
ϵ_0	Dielectric constant of free space (vacuum)
κ_S	Permittivity of semiconductor
κ_{SiO_2}	Permittivity of silicon-di-oxide
κ_D	Permittivity of dielectric
ϕ_B	SB height
ϕ_{Bn}	SB height for electrons
ϕ_{Bp}	SB height for holes
ϕ_{Bp0}	Intrinsic SB height for holes
ϕ_G	Gate potential barrier
ϕ_M	Work function of metal
ϕ_S	Work function of semiconductor
$\phi(y)$	Potential at position Y
ψ_B	Bulk Fermi potential: difference between Fermi Level E_F and intrinsic Fermi Level E_i in bulk region
ψ_{bi}	Build in potential
ψ_{SF}	Surface Potential of Semiconductor
$\psi_{SF,FG}$	Surface potential of semiconductor induced by front gate
$\psi_{SF,BG}$	Surface potential of semiconductor induced by back gate
μ_{eff}	Effective charge carrier mobility

A^{**}	Effective Richardson constant
C_{Dep}	Capacitance contribution of depletion or space charge layer
C_{Ox}	Capacitance contribution of oxide layer
$\mathscr{E}_x$	Electric field
$\mathscr{E}_X$	Electric field in X direction
$\mathscr{E}_Y$	Electric field in Y direction
E_{C}	Energy Level of Conduction Band Bottom Edge
E_{F}	Fermi Energy Level
E_{FM}	Fermi Energy Level of Metal
$E_{\mathrm{FM,D}}$	Fermi Energy Level of Metal at Drain
$E_{\mathrm{FM,S}}$	Fermi Energy Level of Metal at Source
E_{FS}	Fermi energy level of semiconductor
$E_{\mathrm{FS,D}}$	Fermi energy level of semiconductor at drain
$E_{\mathrm{FS,S}}$	Fermi energy level of semiconductor at source
E_{G}	Energy Band Gap of Semiconductor
E_{i}	Intrinsic Fermi Energy level of Semiconductor
E_{V}	Energy Level of Valence Band Top Edge
E_{Vac}	Vacuum Energy Level
G_{m}	Transconductance
$\hbar$	2π-normalized Planck constant, $\hbar = 4.1357\,\mathrm{eVs}$
I_{DS}	Drain-Source Current
$I_{\mathrm{DS,Drive}}$	Drain-Source drive current, i.e. $I_{\mathrm{DS,Drive}} = I_{\mathrm{DS}}(V_{\mathrm{GS}} = V_{\mathrm{DS}})$
$I_{\mathrm{DS,off}}$	Drain-Source Off-State Leakage Current
$I_{\mathrm{DS,CMOS-Off}}$	Drain-Source CMOS Off-State Current, i.e. $I_{\mathrm{DS,CMOS-Off}} = I_{\mathrm{DS}}(V_{\mathrm{GS}} = 0\ V)$
$I_{\mathrm{DS,on}}$	Drain-Source on-state current
J_{FE}	Field emission current density
J_{TE}	Thermionic emission current density

K	Technology factor
k_B	Boltzmann constant
$k_B T$	Thermal energy ($k_B T / q$ thermal voltage)
L_G	Gate length
L_{OV}	Gate overlap
m_0	Free electron rest mass (9.11x^{-31} kg)
m^*	Effective charge carrier mass
m^*_{tn}	Tunneling mass of electrons
m^*_{tp}	Tunneling mass of holes
$N_{A/D}$	Acceptor or donator doping concentration (atoms/cm^{-3})
n_i	Intrinsic charge carrier concentration of a semiconductor
$n_{p,SF}$	Negative minority charge carrier concentration at the surface, i.e. electrons, in p-type semiconductor
$p_{p,SF}$	Positive majority charge carrier concentration at the surface, i.e. holes, in p-type semiconductor
q	Elementary charge
S	Sub-threshold slope
sub-V_{th}	Sub-threshold voltage
t_B	Silicon body thickness
T	Temperature (in Kelvin)
$T_{n,p}$	Tunneling probability for electrons/holes
V_A	Applied voltage
V_{BG}	Back Gate Voltage
V_D	Drain Voltage
V_{DD}	Positive supply voltage in integrated CMOS circuits
V_{DS}	Drain-Source Voltage
V_{FB}	Flatband voltage
V_{FG}	Front gate voltage

V_G	Gate voltage
V_{GS}	Gate-Source voltage
V_S	Source voltage
V_{SS}	Negative supply voltage in integrated CMOS circuits, commonly ground
V_{th}	Threshold voltage
W_{SCR}	Width of space-charge region
W_G	Channel width of MOSFET in Z-direction
Z	Transport energy factor

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Supervised Student Thesises

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Karsten Beckmann, *Simulation und Technologieoptimierung von NiSi Bandlückenmitten S/D Elektroden für neuartige dotierstoff-freie doppel Steuerelektroden MOSFET Bauelemente*

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